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CBCS SCHEME

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BCS302

Third Semester B.E./B.Tech. Degree Examination, June/July 2026
Digital Design and Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Simplify the following Boolean functions using K-map and obtain the simplified Boolean expressions. i) $F_1(A, B, C, D) = \Sigma m (1, 3, 4, 5, 7, 10, 12)$ ii) $F_2 (A, B, C, D) = \Sigma m (5, 8, 9, 10, 11, 12, 13, 14, 15)$	7	L3	CO1
	b.	Simplify the following Boolean expressions using 4-variable maps : $F = \overline{A}\overline{B}\overline{C}\overline{D} + B\overline{C}D + \overline{A}\overline{C}\overline{D} + \overline{A}BCD + AC\overline{D}$	8	L3	CO1
	c.	List out the properties of Boolean algebra.	5	L1	CO1
		OR			
Q.2	a.	Minimize the following function for POS using K-map and realize it by using basic gates. $F = \pi M (0, 1, 2, 6, 11, 12).d(3, 4, 7, 15)$	7	L3	CO1
	b.	Implement the Boolean function : $F(x, y, z) = \Sigma m (0, 1, 3, 5, 6, 7)$ with NAND gates.	8	L3	CO1
	c.	Explain the digital logic gates.	5	L1	CO1
		Module – 2			
Q.3	a.	Design verilog HDL to implement AND gate, using structural data flow and behavioral model.	7	L2	CO2
	b.	Design a BCD to an excess – 3 code converter and draw the logic diagram of the implementation.	8	L2	CO2
	c.	Explain the steps involved in design procedure of a combinational circuit with an example.	5	L1	CO2
		OR			
Q.4	a.	Write VHDL code for 4-bit parallel adder.	7	L2	CO2
	b.	What is Multiplexer? Explain the 8 : 1 multiplexer with the help of logic diagram and corresponding expression.	8	L2	CO2
	c.	What is Latch? Explain the working of SR latch.	5	L2	CO2

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		Module – 3			
Q.5	**a.**	Explain with a neat diagram the connection between the processor and the memory.	**10**	**L2**	**CO3**
	b.	What is Performance Measurement? Explain the overall SPEC rating for the computer in a program suite.	**10**	**L2**	**CO3**
		OR			
Q.6	**a.**	With a neat diagram, analyze the operational concepts of a computer. Give the operating steps.	**10**	**L2**	**CO3**
	b.	With a neat diagram, explain the single bus architecture and IO interface for an input device.	**10**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	What is the DMA Bus Arbitration? Explain the different Bus Arbitration Techniques.	**10**	**L2**	**CO3**
	b.	Explain the following : i) Direct mapping ii) Associative mapping iii) Set Associative mapping functions.	**10**	**L2**	**CO4**
		OR			
Q.8	**a.**	Explain the Memory Hierarchy. Describe the effect of size, cast and speed.	**10**	**L2**	**CO4**
	b.	Differentiate Interrupts and Exceptions. Explain the polling and daisy chain mechanisms in interrupt handling.	**10**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	What is Pipelining? With an example, explain the 4-stage pipelining concept.	**10**	**L2**	**CO5**
	b.	Write and explain the control sequence for the execution of the unconditional branch instruction.	**10**	**L3**	**CO5**
		OR			
Q.10	**a.**	Explain the internal organization of the processor.	**10**	**L3**	**CO5**
	b.	Write and explain the control sequence for the execution of the instruction: ADD (R3), R1.	**10**	**L3**	**CO5**

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