Technological Innovation Management And Entrepreneurship			
Course Code	24EC51	**CIE Marks**	50
Teaching Hours/Week (L: T:P)	3:0:0	**SEE Marks**	50
Credits	3	**Total Marks**	100
Contact Hours	40	**Exam Hours**	03
Examination type (SEE)	Theory		

Prerequisites:

- Basic understanding of engineering fundamentals.
- Basic knowledge of organizational structure and business concepts.
- Interest in innovation, entrepreneurship, and professional development.

Course Objectives:

- Understand basic skills of Management.
- Understand the need for Entrepreneurs and their skills.
- Identify the Management functions and Social responsibilities.
- Analyze economic development, creativity and Innovation.
- Understand the Ideation Process, creation of Business Model, Feasibility Study and sources of funding.

Teaching-Learning Process (General Instructions)

- These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.
- Adopt innovative teaching methods in addition to traditional lecture-based instruction to enhance both theoretical understanding and practical application skills.
- Provide real-life case studies and industry-oriented examples to strengthen conceptual clarity and professional relevance.
- Support and guide students in self-directed learning through recommended readings, structured assignments, and mentoring.
- Assign homework, quizzes, and graded assignments to monitor student progress and reinforce learning outcomes.
- Encourage collaborative and group-based learning activities to enhance creativity, teamwork, and analytical thinking skills.
- Use short video lectures strategically:
    - As an introduction to new topics (pre-lecture engagement)
    - As revision material after classroom sessions (post-lecture reinforcement)
    - To provide additional examples and support for complex or challenging topics
    - As model solutions for selected exercises and case studies

Module-1	**08 Hours**

Management: Nature and Functions of Management – Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management & Administration, Management as a Science, Art & Profession

Text book1: Chapter 1

Planning: Planning-Nature, Importance, Types, Steps and Limitations of Planning; Decision Making – Meaning, Types and Steps in Decision Making.

Text book 1: Chapter 4, 5

Module-2 **08 Hours**

Organizing and Staffing: Organization-Meaning, Characteristics, Process of Organizing, Principles of Organizing, Span of Management (meaning and importance only), Departmentalization, Committees–Meaning, Types of Committees; Centralization Vs Decentralization of Authority and Responsibility; **Staffing**-Need and Importance, Recruitment and Selection Process

Text book 1: Chapters 7, 8 & 11.

Directing and Controlling: Meaning and Requirements of Effective Direction, Giving Orders; Motivation-Nature of Motivation, Motivation Theories (Maslow's Need-Hierarchy Theory and Herzberg's Two Factor Theory); **Communication** – Meaning, Importance and Purposes of Communication; **Leadership**-Meaning, Characteristics, Behavioral Approach of Leadership; **Coordination**-Meaning, Types, Techniques of Coordination; Controlling – Meaning, Need for Control System, Benefits of Control, Essentials of Effective Control System, Steps in Control Process

Text book 1: Chapters 9,15,16,17,18

Module-3 **08 Hours**

Introduction to Technological Innovation-Basic Concepts and Definitions, Innovation Posture, Propensity and Performance, Innovation Measurement, Competitiveness, A Historical and Socio-Technical Perspective on Innovation, Common Frameworks and Typologies to Characterize Innovations, Innovation Process.

Text book 4: Chapter 1

Innovation Systems: The Concept of Innovation Systems-Types of Innovation Systems, Basic Principles of Innovation Systems, Innovation Systems and Simulation Systems, System Dynamics as a Concept, Tool, and Process-Building a System Dynamics Model.

Text book 4:Chapter 5 –section 5.1-5.5

Module-4 **08 Hours**

Social Responsibilities of Business: Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance

Text book 1: Chapter 3

Entrepreneurship: Definition of Entrepreneur, Importance of Entrepreneurship, concepts of Entrepreneurship, Characteristics of successful Entrepreneur, Classification of Entrepreneurs, Myths of Entrepreneurship, Entrepreneurial Development models, Entrepreneurial development cycle, Problems faced by Entrepreneurs and capacity building for Entrepreneurship .

Text book 2: Chapter 2

Module-5 **08 Hours**

Business model – Meaning, designing, analyzing and improvising; Business Plan – Meaning, Scope and Need; Financial, Marketing, Human Resource and Production/Service Plan; Business plan Formats; Project report preparation and presentation; Why some Business Plan fails?

Text book 2: Chapter 8 (Page No 159-164)

Financing and How to start a Business? Financial opportunity identification; Banking sources; Nonbanking Institutions and Agencies; Venture Capital – Meaning and Role in Entrepreneurship; Government Schemes for funding business; Pre launch, L3 Launch and Post launch requirements; Procedure for getting License and Registration; Challenges and Difficulties in Starting an Enterprise

Text book 2: Chapter 7(Page No 147-149), Chapter 5 (Page No 93-99) & Chapter 8(Page No. 166-172)

Project Design and Network Analysis: Introduction, Importance of Network Analysis, Origin of PERT and CPM, Network, Network Techniques, Need for Network Techniques, Steps in PERT, CPM, Advantages, Limitations and Differences.

Text book 3: Chapter 20

Course outcomes(Course Skill Set):

At the end of the course, the student will be able to:

- **CO1:** Understand the fundamental concepts of Management and Entrepreneurship, and identify business opportunities for establishing an enterprise. *(PO-6,7,8,10)*
- **CO2:** Explain the functions of managers and entrepreneurs, along with their social responsibilities. *(PO-6,7,8)*
- **CO3:** Discuss the components involved in developing a business plan and the integration of Corporate Social Responsibility (CSR). *(PO-7,8,9,10,11)*
- **CO4:** Illustrate the importance of creativity, technological innovation, and identification of business opportunities. *(PO-6,7,8,9)*
- **CO5:** Describe various sources of funding and institutions that support entrepreneurial activities. *(PO-6,7,8,9,10)*

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.

The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods, if an assignment is project-based then only one assignment for the course shall be planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

The Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Textbooks:

1. Principles of Management – P.C Tripathi, P.N Reddy, McGraw Hill Education, 6th Edition, 2017. ISBN-13:978-93-5260-535-4.
2. Entrepreneurship Development Small Business Enterprises- Poornima M Charantimath, Pearson Education 2008, ISBN 978-81-7758-260-4.
3. Dynamics of Entrepreneurial Development and Management by Vasant Desai. HPH 2007, ISBN: 978-81-8488-801-2.
4. Innovation and Entrepreneurship Theory, Policy and Practice, - Innovation, Technology, and Knowledge Management , Elias G. Carayannis , Elpida T. Samara ,Yannis L. Bakou, © Springer International Publishing Switzerland 2015, DOI 10.1007/978-3-319-11242-8, ISBN 978-3-319-11241-1.

Reference Books:

1. Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93- 392-2286-4.

Web links and Video Lectures(e-Resources):

1. https://onlinecourses.nptel.ac.in/noc22_mg42/
2. https://onlinecourses.nptel.ac.in/noc21_mg54/
3. https://onlinecourses.nptel.ac.in/noc24_mg121/
4. https://onlinecourses.nptel.ac.in/noc25_mg95/
5. https://onlinecourses.swayam2.ac.in/ntr25_ed87/
6. https://www.runn.io/blog/skills-management
7. https://www.atlassian.com/work-management/project-management

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning:(But are not limited to)

- Conduct and document a survey on the organizational and management structure of an industry or business organization.
- Study and document the roles and responsibilities of managerial-level employees in an organization.
- Identify and prepare documentation related to the application procedures and forms required for starting a business or Small-Scale Industry (SSI).
- Analyze case studies of successful entrepreneurs to understand innovation, leadership, and business strategies.
- Conduct group discussions and presentations on emerging trends in technology management and entrepreneurship.
- Prepare business model proposals or startup ideas based on real-world problems.
- Participate in seminars, workshops, and entrepreneurship awareness programs.

DIGITAL COMMUNICATION			
Course Code	**24EC52**	**CIE Marks**	**50**
Teaching Hours/Week (L: T:P)	**3:2:0**	**SEE Marks**	**50**
Credits	**4**	**Total Marks**	**100**
Contact Hours	**50**	**Exam Hours**	**3**
Examination type (SEE)	**Theory**		

Prerequisites:

- Fundamentals of Signals and Systems
- Basic Probability Theory and Random Processes
- Fourier Series and Fourier Transform Techniques
- Principles of Analog and Digital Communication
- Elementary Linear Algebra and System Modeling

Course objectives:

- Understand the concept of signal processing of digital data and signal conversion to symbols at the transmitter and receiver.
- Compute performance metrics and parameters for symbol processing and recovery in ideal and corrupted channel conditions.
- Understand the principles of spread spectrum communications.
- Understand the basic principles of information theory and various source coding techniques.
- Build a comprehensive knowledge about various Source and Channel Coding techniques.
- Discuss the different types of errors and error detection and controlling codes used in the communication channel.
- Understand the concepts of convolution codes and analyze the codewords using timedomain and transform domain approach.

Teaching-Learning Process (General Instructions)

Teachers can use the following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with BlackBoard
2. ICT based Teaching

Module-1	**10 Hours**

Bandpass Signals to Equivalent Lowpass: Hilbert Transform, Pre-envelopes, Complex envelopes of Band-pass Signals, Canonical Representation of Bandpass signals. Signalling over AWGN Channels- Introduction, Geometric representation of signals, Gram- Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel , Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver.

Text Book1:Section 2.8 to 2.11,7.1 to 7.4

Module-2	10 Hours
Digital Modulation Techniques: Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M–ary PSK, M–ary QAM. Frequency shift keying techniques using Coherent detection: BFSK generation, detection and error probability. BFSK using Noncoherent Detection, Differential Phase Shift Keying. Text Book 1:Section 7.6 to 7.8,7.10 to 7.12	
Module-3	**10 Hours**
Information theory: Introduction, Measure of information, Long dependent sequences, Markov Statistical Model for Information Sources, Entropy and Information rate of Markoff Sources. Encoding of the Source Output, Shannon's Encoding Algorithm, Shannon Fano Encoding Algorithm Source coding theorem, Prefix Codes, Kraft McMillan Inequality property – KMI, Huffman codes , Channel capacity, Channel Capacity of Binary Symmetric Channel, Binary Erasure Channel, Text Book 2: Sections: 2.1,2.2,2.5,3.4,4.5.4.6	
Module-4	**10 Hours**
Error Control Coding: Error Control Using Forward error Correction, Linear Block Codes: Definitions, Matrix Descriptions, Syndrome and its properties, Minimum distance Considerations, Syndrome Decoding, Hamming Codes. Cyclic Codes: Properties, Generator and Parity Check Polynomial and matrices, Encoding, Syndrome computation, Examples. Text Book 2: Sections: 5.1 to 5.7,6.1 to 6.6	
Module-5	**10 Hours**
Convolutional Codes: Golay Codes, BCH Codes ,Convolutional Encoder, Code tree, Trellis Graph and State graph, Recursive systematic Convolutional codes, Optimum decoding of Convolutional codes, Maximum Likelihood Decoding of Convolutional codes: The Viterbi Algorithm, Examples. Text Book 2: Sections: 7.1 to 7.6	

Course outcomes(Course Skill Set):

At the end of the course, the student will be able to:

CO1: Apply the concept of signal conversion to vectors in communication transmission and reception. (PO-1,2,3 PSO-1,2,3)

CO2: Perform the mathematical analysis of digital communication systems for different modulation techniques. (PO-1,2,3 PSO-1,2,3)

CO3: Apply the Source coding and Channel coding principles for the discrete memoryless channels. (PO-1,2,3 PSO-1,2,3)

CO4: Compute the codewords for the error correction and detection of a digital data using Linear Block Code, Cyclic Codes and Convolution Codes. . (PO-1,2,3 PSO-1,2,3)

CO5: Design encoding and decoding circuits for Linear Block Code, Cyclic Codes and Convolution Code. (PO-1,2,3 PSO-1,2,3)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods , if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks. The Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Book:

1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, 2014, ISBN 978-81- 265-4231-4.
2. Muralidhar Kulkami K S, Shivaprakash, "Information theory and Coding wiely India Pvt Ltd, 2015

Reference Books:

1. B.P Lathi, Zhi Ding, "Modern Digital and Analog Communication Systems",4th Edition, Oxford University press, ISBN: 9780198073802, 2017
2. K Sam Shanmugam, "Digital and analog communication systems", Wiley India Pvt. Ltd, 2017, ISBN:978 81-265-3680-1,.
3. K.N Hari Bhat, D. Ganesh Rao, "Information Theory and Coding", Cengage Learning India Pvt Ltd, 2017, ISBN: 93-866-5092-4,.

Web links and Video Lectures(e-Resources):

Principles of Communication Systems Part II, https://onlinecourses.nptel.ac.in/noc19_ee47/preview

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning (but are not limited to)

- Flipped classroom
- Assessment Methods Marks (opt two Learning Activities)
  Quiz

Digital Signal Processing			
Course Code	24EC53	**CIE Marks**	50
Teaching Hours/Week (L:T:P)	3:0:2	**SEE Marks**	50
Credits	04	**Total Marks**	100
Contact Hours	40 hours Theory + 10 Lab Slots	**Exam Hours**	03
Examination Type	IPCC		

Prerequisites

- Knowledge of basic mathematics such as continuous function, discrete function & difference equations.

Course Objectives:

- Preparation: To prepare students with fundamental knowledge/ overview in the field of Digital Signal Processing
- Core Competence: To equip students with a basic foundation of Signal Processing by delivering the basics of Discrete Fourier Transforms, their properties, efficient computations & the design of digital filters.

Teaching-Learning Process

These are sample strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on that topic in the succeeding classes.
10. Give Programming Assignments.

Module -1 **8 Hours**

Discrete Fourier Transform: Frequency Domain sampling and Reconstruction of Discrete Time Signals, The DFT, The DFT as Linear Transformation.

Properties of DFT: Periodicity, Linearity, Circular time shift, Time reversal, Circular frequency shift, Circular convolution, Modulation and Symmetry properties of real valued sequence, Multiplication of two DFTs and Circular Convolution.

Text 1:7.1,7.2,7.3

Module -2 **8 Hours**

Efficient Computation of the DFT- FFT Algorithms: Direct Computation of the DFT, Radix-2 FFT Algorithms: Computation of DFT and IDFT in decimation in time and frequency.

Text 1:8.1,8.1.1,8.1.2,8.1.3

Module -3 **8 Hours**

Design of FIR Filters: Characteristics of practical frequency-selective filters, Symmetric and Antisymmetric FIR filters, Design of Linear-phase FIR (low pass and High pass) filters using windows - Rectangular, Bartlett, Hanning, Hamming and Blackman windows.

Text 1:10.2.1,10.2.2

Module -4 **8 Hours**

Design of IIR Filters: Infinite Impulse response Filter Format, Bilinear Transformation Design Method, Analog Filters using Low pass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth Filter Design (Lowpass and Highpass) using BLT. Text 1:10.3.3,10.3.5
Module -5 **8 Hours**
Structure for FIR Systems: Direct, Cascade and Lattice Phase structures. **Structure for IIR Systems:** Direct, Cascade and Parallel form. Text 1:9.2.1,9.2.2,9.2.4,9.3.1,9.3.3,9.3.4

PRACTICAL COMPONENT OF IPCC: List of Programs to be implemented & executed using any programming languages like OCTAVE,SCILAB (but not limited to).

Sl.No	Experiments
1	Program to generate the following discrete time signals. a) Unit sample sequence, b)Unit step sequence, c) Exponential sequence, d)Sinusoidal sequence, e) Random sequence
2	Program to perform the following operations on signals. a) Signal addition, b) Signal multiplication, c)Scaling, d) Shifting, e)Folding
3	Program to perform convolution of two given sequences (without using built-in function) and display the signals.
4	Consider a causal system $y(n) = 0.9y(n-1) + x(n)$. a) Determine H(z) and sketch its pole zero plot. b) Plot $\|H(e^{j\omega})\|$ and $\angle H(e^{j\omega})$ c) Determine the impulse response h(n).
5	Computation of N point DFT of a given sequence (without using built-in function) and to plot the magnitude and phase spectrum.
6	Using the DFT and IDFT, compute the following for any two given sequences a)Circular convolution b) Linear convolution
7	Verification of Linearity property, circular time shift property & circular frequency shift property of DFT.
8	Develop decimation in time radix-2 FFT algorithm without using built-in functions
9	Design and implementation of digital low pass FIR filter using a window to meet the given specifications

10	Design and implementation of digital high pass FIR filter using a window to meet the given specifications
11	Design and implementation of digital IIR Butterworth low pass filter to meet the given specifications.
12	Design and implementation of digital IIR Butterworth high pass filter to meet the given specifications

Course Outcomes (Course Skill Set):
At the end of the course, the student will be able to:
CO1: Analyse the different types of signals and systems used in digital signal processing.(PO-1,2,3 PSO-1,2,3)
CO2: Compute the response of an LTI system using time and frequency domain techniques.(PO-1,2,3 PSO-1,2,3)
CO3: Develop algorithms for the efficient computations of DFT and IDFT.(PO-1,2,3 PSO-1,2,3)
CO4: Design of digital FIR filters for the given specifications using different window methods.(PO- 1,2, PSO-1,2,3)
CO5: Design of digital IIR digital filters using bilinear transformation method.(PO-1,2,3 PSO-1,2,3)

- **Assessment Details (both CIE and SEE)**
  The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

  The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are 25 marks and that for the practical component is 25 marks.
- **CIE for the theory component of the IPCC**
  25 marks for the theory component are split into 15 marks for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and 10 marks for other assessment methods. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus. Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for 25 marks). The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.
- **CIE for the practical component of the IPCC**
  15 marks for the conduction of the experiment and preparation of laboratory record, and 10 marks for the test to be conducted after the completion of all the laboratory sessions. On completion of every experiment/program in the laboratory, the students shall be evaluated including vivavoce and marks shall be awarded on the same day. The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' writeups are added and scaled down to 15 marks. The laboratory test (duration 02/03 hours) after completion of all the experiments shall be conducted for 50 marks and scaled down to 10 marks. Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC

for 25 marks. The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

- **SEE for IPCC**

  Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

  1. The question paper will have ten questions. Each question is set for 20 marks.
  2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
  3. The students have to answer 5 full questions, selecting one full question from each module.
  4. Marks scored by the student shall be proportionally scaled down to 50 Marks.

  The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

  The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.

  SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.

  The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources

Text Books:

1. Proakis & Manolakis, “Digital Signal Processing - Principles Algorithms & Applications”, 4th Edition, Pearson education, New Delhi, 2007. ISBN: 81-317-1000-9.

Reference Books:

1. Simon Haykin and Barry Van Veen, “Signals and Systems”, 2nd Edition, 2008, Wiley India. ISBN9971-51- 239-4.
2. Sanjit K Mitra, “Digital Signal Processing, A Computer Based Approach”, 4th Edition, McGraw Hill Education, 2017. ISBN:978-1-25-909858
3. Oppenheim & Schaffer, “Discrete Time Signal Processing", PHI, 2003..

Web links and Video Lectures (e-Resources):

1. Digital Signal processing, https://nptel.ac.in/courses/117102060

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning Programming (But are not limited to)

- Quiz
- Mini Projects
- Flipped Class room

Digital Communication Lab			
Course Code	24ECL54	**CIE Marks**	50
Teaching Hours/Week (L: T:P)	0:0:2	**SEE Marks**	50
Credits	01	**Total Marks**	100
Contact Hours	12 Lab slots	**Exam Hours**	3
Examination type (SEE)	Practical		

Prerequisites:

The students should have knowledge on

- Modulation Basics
- Information Theory and Coding

Course Objectives::

- This laboratory course enables students to
- Design of basic digital modulation techniques using electronic hardware.
- Simulation of vector computations and derive the orthonormal basis set using Gram Schmidt procedure.
- Simulate the digital transmission and reception in AWGN channel
- Simulate the digital modulations using software and display the signals and its vector representations.
- Implement the source coding algorithms using a suitable software platform.
- Simulate the channel coding techniques and perform decoding for error detection and correction.

Teaching-Learning Process (General Instructions)

1. Collaborative Learning
2. Demonstration based Teaching
3. Use of Simulation Tools

Sl. No	Experiments
1	Generation and demodulation of the Amplitude Shift Keying signal.
2	Generation and demodulation of the Phase Shift Keying signal.
3	Generation and demodulation of the Frequency Shift Keying signal.
4	Generation of DPSK signal and detection of data using DPSK transmitter and receiver.
5	Gram-Schmidt Orthogonalization: To find orthogonal basis vectors for the given set of vectors and plot the orthonormal vectors.
6	Simulation of binary baseband signals using a rectangular pulse and estimate the BER for AWGN channel using a matched filter receiver.

7	Perform the QPSK Modulation and demodulation. Display the signal and its constellation.
8	Generate 16-QAM Modulation and obtain the QAM constellation.
9	Encoding and Decoding of Huffman code.
10	Encoding and Decoding of binary data using a Hamming code.
11	For a given data, use CRC-CCITT polynomial to obtain the CRC code. Verify for the cases, a) Without error b) With error
12	Encoding and Decoding of Convolution code

Course outcomes(Course Skill Set):

At the end of the course, the student will be able to:

CO1: Design the basic digital modulation and demodulation circuits for different engineering applications.
(PO-1,2,3,4,9,10,PSO-1,2,3)

CO2: Design of optimum communication receivers for AWGN channels.
(PO-1,2,3,4,9,10,PSO-1,2,3)

CO3: Illustration of different digital modulations using the signals and its equivalent vector representations..
(PO-1,2,3,4,9,10,PSO-1,2,3)

CO4: Implement the source coding and channel coding procedures using suitable software..
(PO-1,2,3,4,9,10,PSO-1,2,3)

Assessment Details(both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

ContinuousInternalEvaluation(CIE):

CIE marks forthepracticalcourseare50Marks.

Thesplit-upofCIE marks forrecord/journalandtest are in the ratio 60:40.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments

listed in the syllabus.

- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva- voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to 20 marks (40% of the maximum marks).
- The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course are 50 Marks.

1. SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute.
2. The examination schedule and names of examiners are informed to the university before the Conduction of the examination.
3. These practical examinations are to be conducted between the schedules mentioned in the academic calendar of the University. All laboratory experiments are to be included for practical examination.
4. (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.
5. Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
6. Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners

   General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners) Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero. The minimum duration of SEE is 02 hours

SuggestedLearning Resources:

1. B. P Lathi, Zhi Ding, "Modern Digital and Analog Communication Systems" 4th Edition, Oxford University Press, 2017, ISBJ:978-0-19-947628-2
2. Herbert Taub, Donald L Schilling, Goutam Saha, "Principles of Communication Systems", Mc Graw Hill Education, 2013, ISBN: 978-1-25-902985-1..

Web links and Video Lectures(e-Resources):

- https://www.nptelprep.in/courses/106103016/materials
- https://vlsiresources.com/frontendvlsi/

- http://vlsi-iitg.vlabs.ac.in/
- https://www.edaplayground.com/
- https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice.html
- https://www.youtube.com/watch?v=J4gTC-KFLi8&list=PL4isOTp6hCIdNn_cFSPCDhoSrTvj5m8CE

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Troubleshooting sessions
- Demonstration

FPGA System Design using Verilog			
Course Code	24EC55A	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	4:0:0	**SEE Marks**	50
Credits	04	**Total Marks**	100
Contact Hours	50	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on:

- Basic knowledge of Digital Electronics
- Fundamentals of Verilog HDL concepts

Course Objectives:

This course will enable students to:

- Understand the types of programmable logic devices and building blocks of FPGA and thus implement the design using Xilinx FPGAs.
- Understand the concepts of Advanced Logic design and implementation using Verilog HDL
- Designing different Digital applications using SM chart.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of combinational and sequential circuits
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.
- Give Programming Assignments.

Module-1	10 Hours
Introduction to Programmable Logic Devices: Overview of Digital System Design Flow, FPGA Architecture Overview, FPGA Design Flow, Basic Timing Concepts, Brief overview of Programmable Logic Devices, Simple Programmable Logic Devices (SPLDs), Complex Programmable Logic devices (CPLDs), Field-Programmable Gate Arrays (FPGAs) Text 1: 1.1 to 1.5	
Module-2	**10 Hours**
Advanced Digital Design Examples: BCD to 7-Segment Display Decoder, BCD Adder, Traffic Light Controller, Synchronization and debouncing, Shift-and-Add Multiplier, Array Multiplier, Keypad Scanner (Excluding Test Bench) Text 1: 3.1 to 3.4, 4.1to 4.5	
Module-3	**10 Hours**
SM Charts and Microprogramming: State Machine Charts, Derivation of SM Charts, SM chart for binary multiplier, Dice Game (Excluding Test Bench), Realization of SM Charts, Implementation of the Dice Game. Microprogramming, Linked State Machines. Text 1: 5.1 to 5.5, 6.1, 6.2	
Module-4	**10 Hours**
Arithmetic Circuits, Primitives, Memory modeling: Fixed vs Floating Point Representation, Floating Point Addition, Arithmetic Design Consideration, Gate-Level Modelling, User Defined Primitives, Multi-valued Logic, Delay Modelling, SRAM Modelling, Read/Write Operations, Timing Constraints Text 1: 7.1 to 7.3, 8.1 to 8.4, 9.1 to 9.3	
Module-5	**10 Hours**
Designing with Field Programmable Gate Arrays: Implementing Functions in FPGAs, Implementing Functions Using Shannon's Decomposition, Carry Chains in FPGAs, Cascade Chains in FPGAs, Examples of Logic Blocks in Commercial FPGAs, Dedicated Multipliers in FPGAs, FPGAs Capacity: Maximum gates versus Usable gates, Design Translation. Text 1: 10.1 to 10.5, 11.1 to 11.3	

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Apply the concepts of Programmable Logic Devices (SPLDs, CPLDs, FPGAs) to implement digital designs. (PO – 1,2 , PSO –1)

CO2: Design and implement advanced digital circuits using Verilog HDL.
(PO – 1,3, PSO – 1,2)

CO3: Analyze and design complex digital systems using State Machine (SM) Charts and microprogramming techniques. (PO – 2,3, PSO – 1,2)

CO4: Perform floating-point arithmetic operations and model memory systems using Verilog.

(PO – 1,2, PSO – 1)

CO5: Design, implement, and evaluate advanced digital systems using FPGA architecture features. (PO – 2,3,4, PSO – 1,2)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks).
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with 3. a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books

1. Pong P. Chu, FPGA Prototyping by Verilog Examples, 2nd Edition (Zynq Version), Wiley, 2022. ISBN: 978-1119282662

Reference Books:

1. Advanced FPGA Design Architecture, Implementation, and Optimization Steve Kilts Spectrum
2. ASIC and FPGA Verification: A guide to component Modelling. Richard Munden, Morgan Kaufmann Publishers is an imprint of Elsevier.
3. Processor Design, System-on-Chip Computing for ASICs and FPGAs, Jari Nurmi Finland Tampere University of Technology Sringer Publications.
2. Digital Systems Design Using Verilog, First Edition, Charles H. Roth, Jr. The University of Texas at Austin, Lizy Kurian John, The University of Texas at Austin, Byeong Kil Lee, The University of Texas at San Antonio.

The design Warrior's guide to FPGA Clive 'Max' Maxfield Elsevier Publications

Web links and Video Lectures(e-Resources):

- **http://acl.digimat.in/nptel/courses/video/117105080/L13.html**
- **https://onlinecourses.nptel.ac.in/noc25_ee24/**
- **https://www.youtube.com/watch?v=VtbPexCocVo&list=PLbFgDf51ZkCEJb9MvxKIs-0q2obouwf-f&index=1**
- **https://www.youtube.com/watch?v=XCLmatskK5w&list=PLwdnzlV3ogoVlY7iVqr-FhWUQEX7JDdiP&index=32**
- **https://www.youtube.com/watch?v=t6-Jt1CD9cc&list=PLwdnzlV3ogoVlY7iVqr-FhWUQEX7JDdiP&index=39**

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Role Play
- Flipped classroom
- Assessment Methods for 25 Marks (opt two Learning Activities)
  - Programming Assignment
  - Group Discussion/Quiz.
  - Demonstration of Verilog and FPGA concepts.
  - Case Study on small design and implementation on FPGA's.

Intelligent Systems with Machine Learning Algorithms			
Course Code	24EC55B	**CIE Marks**	50
Teaching Hours/Week (L: T:P)	4:0:0	**SEE Marks**	50
Credits	04	**Total Marks**	100
Contact Hours	50	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on basic of programming

Course Objectives:

- Gain a historical perspective of AI and its foundations.
- Become familiar with basic principles of AI toward Problem-Solving
- Get to know approaches of inference, perception, knowledge representation, and learning
- Define Machine Learning and understand the basic theory underlying machine learning.
- Differentiate supervised, unsupervised, and reinforcement learning

Teaching-Learning Process (General Instructions)

These are sample Strategies teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method; different teaching methods may be adopted to develop the outcomes.

2. Encourage collaborative (Group) Learning in the class.

3. Ask at least three HOTS (Higher Order Thinking) questions in the class, which promotes critical thinking.

4. Adopt Problem-Based Learning (PBL), which fosters students' Analytical skills, and develops thinking skills such as evaluating, generalizing, and analyzing information rather than simply recalling it.
5. Topics will be introduced in a multiple representation.

6. Show the different ways to solve the same problem and encourage the students to come up with creative ways to solve them.

7. Discuss how every concept can be applied to the real world and when that's possible, it helps improve the student's understanding. 8. Adopt the Flipped class technique by sharing the materials/Sample Videos before the class and having discussions on the topic in the succeeding classes.

Module-1	10 Hours
Introduction: What is AI? Foundations and History of AI Intelligent Agents: Agents and environment, Concept of Rationality, The nature of environment, The structure of agents. **Text book 1: Chapter 1- 1.1, 1.2, 1.3 Chapter 2- 2.1, 2.2, 2.3, 2.4**	
Module-2	**8Hours**
Problem-solving: Problem-solving agents, Example problems, Searching for Solutions Uninformed Search Strategies: Breadth First search, Depth First Search, Iterative deepening depth first search **Text book 1: Chapter 3- 3.1, 3.2, 3.3, 3.4**	
Module-3	**10 Hours**
Introduction to State Space Search and Problem Formulation**,** Uninformed vs. Informed Search – Comparative Analysis**,** Informed (Heuristic) Search Techniques**,**Heuristic Functions: Design, Admissibility, and Consistency**,** Performance Metrics of Search Algorithms (Time & Space Complexity)**,** Greedy Best-First Search: Algorithm and Limitations**,** A* Search: Evaluation Function, Optimality, and Completeness**,**Memory-Bounded Heuristic Search (IDA*, RBFS – Overview)**,** Knowledge-Based Agents: Structure and Working Principle**,** Knowledge Representation Techniques**,** The Wumpus World: PEAS Description and Environment Properties,Foundations of Logic in Artificial Intelligence Syntax and Semantics of Propositional Logic**,**Normal Forms (CNF & DNF) in Propositional Logic**,**Inference Rules: Modus Ponens, Modus Tollens, Resolution**,**Entailment, Validity, and Logical Equivalence**,**Limitations of Propositional Logic and Introduction to First-Order Logic (Overview) **Text book 1: Chapter 3-3.5,3.6 Chapter 4 – 4.1, 4.2 Chapter 7- 7.1, 7.2, 7.3, 7.4, 7.5**	
Module-4	**10 Hours**
Introduction: Machine learning Landscape: what is ML?, Why, Types of ML, main challenges of ML Concept learning and Learning Problems – Designing Learning systems, Perspectives and Issues – Concept Learning – Find S-Version Spaces and Candidate Elimination Algorithm – Remarks on VS-Inductive bias**.** **Text book 3: Chapter 1, Textbook 4:Chapter 1, 2**	
Module-5	**10 Hours**
End-to-end Machine learning Project: Working with real data, Look at the big picture, Get the data, Discover and visualize the data, Prepare the data, select and train the model, Fine tune your model. Classification: MNIST, training a Binary classifier, performance measure, multiclass classification, error analysis, multi-label classification, multi-output classification **Text book 4: Chapter 2, 3**	
Course outcomes(Course Skill Set): At the end of the course, the student will be able to: CO 1: Apply knowledge of agent architecture, searching, and reasoning techniques for different	

Applications..(PO –1,2,3PSO –1)
CO 2: Compare various Searching and Inferencing Techniques.(PO–1,2,3PSO –1)
CO 3: Develop knowledge base sentences using propositional logic and first-order logic(PO–1,2,3PSO – 1)
CO 4: Understand the concept of Machine Learning and Concept Learning. PO– 1,2,3PSO – 1)
CO 5: Apply the concept of ML and various classification methods in a project (PO–1,2,3 PSO –1)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)

The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

The Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination: Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.

2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module**.**

3. The students have to answer 5 full questions, selecting one full question from each module.

Suggested Learning Resources:

Textbook:

1. Stuart J. Russell and Peter Norvig , Artificial Intelligence, 3rd Edition, Pearson,2015
2. Elaine Rich, Kevin Knight, Artificial Intelligence, 3rd Edition,Tata McGraw Hill,2013.
3. Tom M. Mitchell, Machine Learning, McGraw-Hill Education, 2013
4. Aurelien Geron, Hands-on Machine Learning with Scikit-Learn &Tensor Flow , O'Reilly, Shroff Publishers and Distributors Pvt. Ltd 2019.

Reference Books:

1. George F Lugar, Artificial Intelligence Structure and strategies for complex, Pearson Education, 5th Edition, 2011
2. Nils J. Nilsson, Principles of Artificial Intelligence, Elsevier, 1980
3. Saroj Kaushik, Artificial Intelligence, Cengage learning,
4. Ethem Alpaydin, Introduction to Machine Learning, PHI Learning Pvt. Ltd, 2nd Ed., 2013
5. T. Hastie, R. Tibshirani, J. H. Friedman, The Elements of Statistical Learning, Springer, 1st edition, 2001
6. Machine Learning using Python, Manaranjan Pradhan, U Dinesh Kumar, Wiley, 2019
7. Machine Learning, Saikat Dutt, Subramanian Chandramouli, Amit Kumar Das, Pearson,2020

Web links and Video Lectures(e-Resources):

- NPTEL Video lectures: https://nptel.ac.in/courses/106105077
- NPTEL Video lectures: https://nptel.ac.in/courses/106102220
- https://archive.nptel.ac.in/courses/106/105/106105152 https://archive.nptel.ac.in/courses/106/106/106106202
- https://nptel.ac.in/domains/discipline/106?course=106

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning but not limited to

- Group Discussion/Quiz
- Mini projects**.**

Embedded Programming			
Course Code	24EC55C	**CIE Marks**	50
Teaching Hours/Week (L: T:P)	4:0:0	**SEE Marks**	50
Credits	4	**Total Marks**	100
Contact Hours	40	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

Basics of C programming

Course Objectives:

- Comprehend the fundamentals of programming and embedded systems concepts.
- Develop programming skills using Embedded C and Embedded C++.
- Understand control structures, functions, data handling, and I/O operations in embedded systems.
- Understand interfacing of peripherals and implementation of interrupts in microcontroller-based systems.
- Introduce students with debugging techniques, modern engineering tools, and project management concepts.

Teaching-Learning Process (General Instructions)

Teachers can use the following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Project based on activity Teaching

Module-1 **8 Hours**

Introduction to Programming

Introduction, history of programming, various programming languages, frontend,backend programming,human and machine interaction

Text book 1 : Chapter 16

Module-2 **8 Hours**

Embedded Programming

Introduction, Embedded C and C ++ programming,Writing first embedded program,Control structure and

decision making,Datatypes in embedded C and C++,Variables,Functions.

Text Book 1:17 & 18

Module-3 **8 Hours**

Basics of Embedded Programming

Input output operations,Standard Input and Output(I/O) library functions,Interfacing with hardware components for I/O operations,Interrupts and I/O operations.

Text Book 1: Chapter 19

Module-4 **8 Hours**

Advance Embedded Programming

Embedded programming for microcontroller,Peripheral interfacing with embedded C, Debugging embedded C and C++ program,Timing and delay techniques,Interrupt latency and response time.

Text Book 1: Chapter 20

Module-5 **8Hours**

Tools and Project Management

Introduction,Modern engineering tools, Computer circuit simulation,IDE,Computer aided drawing,Introduction to project management

Text Book 1: Chapter 23

Course outcomes(Course Skill Set):

At the end of the course, the student will be able to:
CO1: Explain basic programming concepts and embedded system fundamentals (PO – 1,2, PSO –1,2)
CO2: Develop embedded programs using Embedded C and Embedded C++ (PO–1,2,5 PSO –1,2)
CO3: Implement input/output operations and interrupt handling in embedded applications. (PO–1,2,3 PSO – 1)
CO4: Interface peripherals and apply debugging techniques in embedded systems. (PO– 1,2,3 PSO –1)
CO5: Use modern engineering tools, IDEs, and project management practices for embedded system development. (PO– 1,2,5 PSO – 1)

Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation)

and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks

The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks

- Any two assignment methods, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 marks will be the sum of the scale-down marks of tests and assignment/s marks. The Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course. Semester-End Examination: Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.

2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.

3. The students have to answer 5 full questions, selecting one full question from each module. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Book:

1.Electrical Engineering Embedded Systems for Engineers and Students, Sheikh Muhammad Ibraheem and Sadia Adrees, Kindle Edition, May 2023, ISBN 978-9692386302.

Reference Book:

1.Embedded system programming with C++ real world techniques, Robert Johnson, Kindle Edition, 10 November 2024, ISBN-13 979-8896650119.

Web links and Video Lectures(e-Resources):

- http://www.digimat.in/nptel/courses/video/117106113/L01.html
- https://onlinecourses.nptel.ac.in/noc20_ee98/

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning (but not limited to)

- Case Study
- Programming Assignment
- Gate Based Aptitude Test

Satellite and Optical Communication			
Course Code	**24EC55D**	**CIE Marks**	**50**
Teaching Hours/Week (L: T:P)	**4:0:0**	**SEE Marks**	**50**
Credits	**04**	**Total Marks**	**100**
Contact Hours	**50**	**Exam Hours**	**3**
Examination type (SEE)	**Theory**		

prerequisites:

Students should have strong knowledge in the following areas.

- Electromagnetic theory
- Analog and Digital Communication
- Signals and Systems

Course objectives:

- Understand the basic principles of satellite orbits and trajectories
- Study of electronic systems associated with a satellite and the earth station.
- Understand the various technologies associated with the communication satellite.
- Learn the basic principle of optical fiber communication with different modes of light propagation.
- Understand the transmission characteristics and losses, optical components and its applications in optical communication.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1	**10 Hours**

Satellite Orbits and Trajectories: Definition, Basic Principles, Orbital parameters, Injection velocity and satellite trajectory, Types of Satellite orbits, Orbital perturbations, Satellite stabilization, Orbital effects on satellite‘s performance, Eclipses, Look angles: Azimuth angle, Elevation angle.

Text book 1: 2.1,2.2,2.3,2.4,2.5,3.3,3.4,3.5,3.6,3.7

Module-2	**10 Hours**

Satellite subsystem: Power supply subsystem, Attitude and Orbit control, Tracking, Telemetry and command subsystem, Payload.

Earth Station: Types of earth station, Architecture, Design considerations, Testing, Earth station Hardware, Satellite tracking.

Text book 1: 4.1,4.5,4.6,4.7,4.8, 8.1,8.2,8.3,8.4,8.5,8.6,8.7

Module-3	**10 Hours**

Communication Satellites: Introduction, Related Applications, Frequency Bands, Payloads, Satellite Vs. Terrestrial Networks, Satellite Telephony, Satellite Television, Satellite radio, Regional satellite Systems, National Satellite Systems.

Text book 1: 9.1,9.2,9.3,9.4,9.5,9.6,9.7,9.8,9.10

Module-4 10 Hours
Optical Fiber Structures: Optical Fiber Modes and Configurations, Mode theory for circular waveguides, Single mode fibers, Fiber materials. Attenuation and Dispersion: Attenuation, Absorption, Scattering Losses, Bending loss, Signal Dispersion: Modal delay, Group delay, Material dispersion. Text book 2 : 2.3,2.3.1 to 2.3.4, 2.4,2.4.1, 2.4.2,,2.5, 2.7,3.1, 3.2
Module-5
Optical Sources and detectors: Light Emitting Diode: LED Structures, Light source materials, Quantum efficiency and LED power, Laser Diodes: Modes and threshold conditions, External quantum efficiency, Resonant frequencies, Photodetectors: The pin Photodetector, Avalanche Photodiodes. **Optical Amplifiers**: Optical amplifiers, basic applications and types, semiconductors optical amplifiers, EDFA **WDM Concepts:** Overview of WDM, Isolators and Circulators, Fiber grating filters (No derivation) Text book 2: 4.2 ,4.3, 6.1, 10.1, 10.3, 10.4, 10.5, 10.7
Course Outcomes(Course Skill Set): **At the end of the course, the student will be able to:** **CO1:** Describe the satellite orbits and its trajectories with the definitions of parameters associated with it**(PO-1, 2, 3, 5 PSO-1, 2)** **CO2:** Describe the Electronic hardware systems associated with the satellite subsystem and earth station. **(PO-1, 2,3, PSO-1,2)** **CO3:** Describe the communication satellite with the focus on the national satellite system. **(PO-1, 2, PSO-1,2)** **CO4:** Classification and characterization of optical fibers with different modes of signal propagation. **(PO-1,2,3 PSO-1,2)** **CO5:** Evaluate and select appropriate optical sources, detectors, amplifiers, and WDM techniques for designing efficient fiber optic communication systems.**. (PO-1,2,3,5, PSO-1,2)**

Assessment Details (Both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignments, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

The Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**
2. The question paper will have ten questions. Each question is set for 20 marks.
3. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

4. The students have to answer 5 full questions, selecting one full question from each module.
5. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Book:

1. Anil K. Maini, Varsha Agrawal, Satellite Communications, Wiley India Pvt. Ltd., 2015, ISBN: 978-81-265-2071-8.
2. Gerd K Kieser,Optical Fiber Communication, 5th Edition, McGraw Hill Education (India) Private Limited, 2016. ISBN:1-25-900 687-5.

Reference Books :

1. Dennis Roddy, Satellite Communications, 4th Edition, McGraw- Hill International edition, 2006
2. Timothy Pratt, Charles Bostian, Jeremy Allnutt, Satellite Communications, 2nd Edition, Wiley India Pvt. Ltd , 2017, ISBN: 978-81-265-0833-4
3. John M Senior, Optical Fiber Communications, Principles and Practice, 3rd Edition, Pearson Education, 2010, ISBN:978-81-317-3266-3
4. Fiber optic communication – Joseph C Palais: 4th Edition, Pearson Education.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/courses/117105131
- Basic Introduction To Satellite Communications | Satellite Communications - YouTube
- How Satellite Works (Animation) - YouTube
- Introduction video: Fiber Optic Communication Technology (youtube.com)

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning(but are not limited to):

- Seminar
- Flipped classroom
- Quiz

Functional Verification using System Verilog			
Course Code	24EC56A	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	3:0:0	**SEE Marks**	50
Credits	04	**Total Marks**	100
Contact Hours	50	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Fundamentals of Digital Electronics and Logic Design
- Knowledge of HDL concepts (Verilog/VHDL basics)
- Basic understanding of VLSI Design flow
- Familiarity with CMOS digital circuits
- Basic programming concepts (C/C++ or similar procedural language)
- Understanding of simulation concepts and digital system modelling.

Course Objectives:

1. Understand verification concepts and System Verilog features used in functional verification.
2. Apply System Verilog constructs for building verification environments.
3. Develop object-oriented verification components.
4. Implement constrained random verification and coverage techniques.
5. Understand modern verification methodologies including UVM basics.

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Demonstration based Teaching

Module-1 **10 Hours**

Introduction to Functional Verification

Verification concepts and need for verification, design flow vs verification flow, verification methodologies, simulation-based verification, directed testing and constrained random testing, coverage-driven verification, HDL vs HVL, overview and features of SystemVerilog, SystemVerilog design and verification environment.

Chapter1,2,3 of Text Book 1

Module-2	10 Hours
SystemVerilog Fundamentals for Verification SystemVerilog data types (2-state and 4-state), arrays (static, dynamic, associative, queues), structures and unions, procedural statements, tasks and functions, packages, interfaces and modports, clocking blocks and synchronization concepts. Chapter2,4,5 of Text Book 1	
Module-3	**10 Hours**
Object-Oriented Programming in SystemVerilog Classes and objects, class members, constructors, encapsulation, inheritance, polymorphism, virtual methods, abstract classes, communication mechanisms — mailbox and semaphore, process synchronization techniques. Chapter6,7,8 of Text Book 1	
Module-4	**10 Hours**
Constrained Random Verification and Coverage Randomization concepts, rand and randc variables, constraint blocks, inline constraints, constraint control, functional coverage concepts, covergroups, coverpoints, cross coverage, introduction to assertions — immediate and concurrent assertions. Chapter6,9,10 of Text Book 1	
Module-5	**10 Hours**
Advanced Verification Methodology Verification environment architecture, transaction-level modeling (TLM), testbench components — generator, driver, monitor, scoreboard, verification planning, regression testing, debugging strategies, introduction to Universal Verification Methodology (UVM), overview of UVM components and phases. Chapter11,12,13 of Text Book 1	

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Explain functional verification concepts and SystemVerilog fundamentals.
. (PO – 1,2 PSO – 5)

CO2: Apply SystemVerilog constructs to build verification environments.
(PO – 1,2,3, PSO – 1,2)

CO3: Develop object-oriented verification components using SystemVerilog..
(PO – 1,2,3, PSO – 1,2)

CO4: Implement constrained random verification and functional coverage techniques.
(PO – 1,2,3,PSO – 1,2)

CO5: Understand advanced verification methodologies and UVM framework.
(PO – 1,2,3, PSO – 1,2)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the regulations; if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Textbook:

1. **Chris Spear and Greg Tumbush**, SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Springer, 3rd Edition.

2. **Janick Bergeron**, Writing Testbenches using SystemVerilog, Springer, 2nd Edition.

Reference Books:

1 **Stuart Sutherland, Simon Davidmann and Peter Flake**, SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling, Springer.

2. **Ashok B. Mehta**, Digital VLSI Design and Verification, McGraw Hill Education.

3. **Mentor Graphics**, UVM Cookbook (Universal Verification Methodology User Guide).

4. **IEEE Standard 1800**, SystemVerilog Language Reference Manual (LRM).

Web links and Video Lectures(e-Resources):

- **SystemVerilog Tutorials & Verification Articles**
  https://www.systemverilog.io/
- **ASIC / SoC Verification Learning Portal**
  https://www.systemverilog.io/verification/
- **Accellera UVM Tutorial (Official Resource)**
  https://www.accellera.org/resources/videos/uvm-tutorial-2014
- **Design Verification with SystemVerilog & UVM – Course Overview**
  https://studybullet.com/course/design-verification-with-systemverilog-uvm/
- **SystemVerilog Verification Training Content (Maven Silicon)**
  https://elearn.maven-silicon.com/course/SystemVerilogforVerification-107

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Role Play
- Flipped classroom
- Assessment Methods for 25 Marks (opt two Learning Activities)
  - Case Study
  - Assignment & online certifications
  - Simulation of circuits using suitable software

Digital Image Processing			
Course Code	24EC56B	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	(4:0:0)	**SEE Marks**	50
Credits	4	**Total Marks**	100
Contact Hours	50	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on:

Linear algebra (matrices/vectors), calculus, probability/statistics, and discrete signal processing (Fourier transforms, convolution).

Course Objectives:

- Understand the fundamentals of digital image processing.
- Apply spatial domain enhancement techniques.
- Analyze image transforms in frequency domain.
- Understand color image processing techniques.
- Design basic image restoration techniques.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Show Video/animation films to explain the functioning of various image processing concepts
2. Encourage cooperative (Group) Learning through puzzles, diagrams, coding etc., in the class.
3. Encourage students to ask questions and investigate their own ideas helps improve their problem-solving skills as well as gain a deeper understanding of academic concepts.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Students are encouraged to do coding based projects to gain knowledge in image processing.
6. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
7. Topics will be introduced in multiple representations.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding
9. Arrange visits to nearby PSUs such as CAIR (DRDO), NAL, BEL, ISRO, etc., and small-scale software industries to give industry exposure.

Module-1	**10 Hours**

Digital Image Fundamentals: What is Digital Image Processing? Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels.

Text book 1: Chapter 1, Chapter 2: Sections 2.1 to 2.5]

Module-2	10 Hours

Spatial Domain: Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters

Text book 1: Chapter 3: Sections 3.2 to 3.6

Module-3	10 Hours

Image Transforms :

Introduction,need for transform,Image transforms,2D-DFT, Properties of 2D-DFT,Walsh Transform, Hadamard Transform

Self Study: DCT and Haar Transform

Text book 2: Chapter 4: Sections 4.1,4.2,4.3,4.5,4.6,4.8,4.9

Module-4	10 Hours

Frequency Domain: Basics of Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters. Color Image Processing: Color Fundamentals, Color Models, Pseudo-color Image Processing.

Text book 1: Chapter 4: Sections 4.7 to 4.9 and Chapter 6: Sections 6.1 to 6.3

Module-5	10 Hours

Restoration: A model of the Image Degradation/Restoration Process, Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering.

Text book 1: Chapter 5: Sections 5.1, to 5.4.3, 5.7, 5.8

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Explain fundamentals of digital image formation and sampling.(PO-1,2 PSO-1,2)

CO2: Apply spatial enhancement techniques.(PO-1,2 PSO-1,2,3)

CO3: Analyze and compute frequency domain transforms.(PO-1,2 PSO-1,2,3)

CO4: Implement color image processing methods.(PO-1,2 PSO-1,2,3)

CO5: Design basic image restoration techniques.(PO-1,2 PSO-1,2,3)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)

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Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text book:

1. Digital Image Processing- Rafael C Gonzalez & Richard E Woods,3rd Edition
2. Digital Image Processing-S.Jayaraman,S.Esakkirajan,T.Veerakumar-Tata McGraw Hill,3rd Reprint, 2010

Reference book:

1. Fundamentals of Digital Image Processing- A K Jain, PHI Learning Private Limited 2014

Web links and Video Lectures(e-Resources):

- Image databases, https://imageprocessingplace.com/root_files_V3/image_databases.htm
- Student support materials, https://imageprocessingplace.com/root_files_V3/students/students.htm
- NPTEL Course, Introduction to Digital Image Processing, https://nptel.ac.in/courses/117105079
- Computer Vision and Image Processing, https://nptel.ac.in/courses/108103174

- Image Processing and Computer Vision – Matlab and Simulink,
- https://in.mathworks.com/solutions/image-video-processing.htm

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning(But are not limited to)

- Role Play
- Flipped classroom
- Case Study
- Programming Assignment
- Gate Based Aptitude Test

IoT Communication Protocols			
Course Code	24EC56C	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	4:0:0	**SEE Marks**	50
Credits	04	**Total Marks**	100
Contact Hours	50	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge of

- **Microcontrollers and Embedded Systems**
- **Programming Skills**

Course Objectives:

- Understand fundamentals of IoT architecture outline and standards.
- Understand and analyze different IoT Networking Technologies
- Understand the importance of different layer Protocols in IoT
- Understand the importance of IIoT & its Protocols.
- Understand the importance of architecture and Industrial Internet of Things

Teaching-Learning Process (General Instructions)

Teachers can use the following strategies to accelerate the attainment of the various course outcomes.

1. **Conceptual Teaching using Chalk and Board**
   Explain fundamental concepts such as protocol architecture, layering, and working principles of protocols like MQTT, CoAP, HTTPetc using diagrams and flowcharts.
2. **ICT-Based Teaching**
   Utilize presentations, simulation tools, and online platforms to demonstrate protocol operations, packet flow, and real-time communication in IoT systems.
3. **Problem-Based Learning**
   Engage students with real-world scenarios such as smart home systems or industrial IoT applications, where they analyze and select suitable communication protocols.
4. **Demonstration-Based Teaching**
   Demonstrate working models using IoT kits (e.g., Raspberry Pi, Arduino) to show practical implementation of communication protocols like MQTT or Bluetooth.

Module-1	**10 Hours**

Fundamentals of IoT :

Introduction: IoT Technology trends and future opportunities, IoT and Business scope Evolution, Business perspectives, Embedded systems Relationships, Challenges of IoT, Characteristics of IoT, Sensors and Actuators in IoT enabling Industrial Automation, Wireless sensor Networks in IoT, Connecting all the things in Internet of things ,IoT M2M, Software Define Networking. IoT System Management is Essential.

Text Book : **Ch1, 1.1-1.13**

Module-2 **10 Hours**

IoT protocols

Introduction IOT life cycle , Physical Design, IOT Conceptual architecture, IOT protocols, Levels of IOT, IOT networking Protocols , Networking standards and technologies in IOT

Text Book : **Ch.3 3.1-3.8**

Module-3 **10 Hours**

IoT protocols

Introduction of 5G networks in IoT, IoT Networking consideration and Challenges, Business case for the IoT, Network optimization for IoT devices,Transport Layer protocols, Network Layer Protocols, IoT communication Challenges, Application Protocols for IoT.

Text Book : Ch.3, 3.9-3.17.

Module-4 **10 Hours**

IIOT

Introduction, Evolution of IIOT, Advantages of IIOT, Drivers, Risk associated with IIOT, Businesses and Industries approach IIOT security , Applications of IIOT, Work flow of IIOT, Security considerations and challenges, IIOT : Use Cases

Text Book : Ch.4, 4.1-4.11

Module-5 **10 Hours**

Architecture of IIOT

Introduction, IIOT layered Architecture ,Three tier IIOT, Security in IIOT, Service based Frameworks, Solutions against Intrusions in IIOT, Machine learning based solutions, Deep Learning based solutions

Text Book: Ch.5, 5.1-5.9

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Describe fundamentals of IoT architecture outline and standards. (PO – 1,2 PSO – 1,2,3)

CO2: Analyse different IoT Networking Technologies (PO – 1,2 PSO – 1,2,3)

CO3: Comprehend the importance of different layer Protocols in IoT (PO – 1,2 PSO – 1,2,3)

CO4: Develop an understanding of the importance of IIoT & its Protocols(PO – 1,2 PSO – 1,2,3)

CO5: Analyse the architecture and Industrial Internet of Things (PO – 1,2 PSO – 1,2,3)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and

for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the college as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Book:

1.Dr. Vijendra Pratap Singh, Mr. Neeraj Kumar.., "IoT Communication Protocols", ISBN: 978-81-961690-9-1,Deccan International Academic Publishers,2023.

Reference Books:

1. Bernd Scholz-Reiter, Florian Michahelles, "Architecting the Internet of Things", ISBN 978-3-642-19156-5 e-ISBN 978-3-642-19157-2, Springer, 2016.
2. N. Ida, Sensors, Actuators and Their Interfaces, Scitech Publishers, 2014.

Web links and Video Lectures(e-Resources):

- https://onlinecourses.nptel.ac.in/noc19_cs65/preview
- https://archive.nptel.ac.in/courses/106/105/106105166/
- https://onlinecourses.nptel.ac.in/noc21_ee85/preview

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Flipped classroom
- Case Studies
- Programming Assignment
- Certification course

RADAR Systems			
Course Code	24EC56D	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	(3:0:0)	**SEE Marks**	50
Credits	3	**Total Marks**	100
Contact Hours	50	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on;

Basic knowledge of **Electromagnetic Theory, Microwave Engineering, Signals and Systems, Communication Systems, Probability and Random Processes, and Electronic Devices & Circuits** is required.

Students should be familiar with wave propagation, Fourier transforms, modulation techniques, noise analysis, and basic amplifier/oscillator circuits.

Course Objectives:

· **To understand the basic principles of radar systems**, including radar range equation, detection concepts, and electromagnetic wave propagation.

· **To analyze different radar system components** such as transmitters, receivers, duplexers , antennas, and displays.

· **To study various radar waveforms and signal processing techniques**, including pulse radar, CW radar, MTI, and Doppler radar.

· **To understand radar detection theory**, noise effects, SNR, probability of detection, and false alarm concepts.

· **To explore advanced radar systems**, such as phased array radar, tracking radar, and synthetic aperture radar (SAR).

· **To apply radar concepts in practical applications**, including navigation, surveillance, weather monitoring, defense, and aerospace systems.

Teaching-Learning Process (General Instructions)

1. **Chalk & Talk / PowerPoint Lectures**
Explanation of radar fundamentals, radar range equation, detection theory, and system components using board illustrations and presentations.

2. **Problem-Solving Sessions**
Numerical problems on radar range equation, Doppler shift, SNR, and probability of detection to strengthen analytical

skills.

3.**Simulation-Based Learning**
MATLAB/Python simulations for radar signal processing, pulse compression, MTI, and Doppler radar concepts.

4.**Case Studies & Applications**
Study of real-world radar systems used in aviation, weather monitoring, marine navigation, and defense.

5.**Laboratory Demonstrations (if available)**
Demonstration of microwave components, antennas, and radar subsystems.

6.**Seminars / Technical Presentations**
Student presentations on advanced topics like phased array radar, synthetic aperture radar (SAR), and tracking radar.

7.**Assignments & Mini Projects**
Design-oriented and analytical tasks to apply theoretical knowledge.

Module-1	**10 Hours**

Basics of Radar:

Introduction, Maximum Unambiguous Range, Radar Waveform, Definitions with respect to pulse wave form- PRF,PRI, Duty Cycle, Peak Transmitter Power, Average transmitter Power. Simple form of the Radar Equation, Radar Block Diagram and Operation, Radar Frequencies, Applications of Radar, The Origins of Radar, Illustrative Problems

[Text 1: Chapter 1, Chapter 2]

Module-2	**10 Hours**

The Radar Equation:

Prediction of Range 'Performance, Detection of signal in Noise, Minimum Detectable Signal, Receiver Noise, SNR, Modified Radar Range Equation, Envelope Detector - False Alarm Time and Probability, Probability of Detection, Radar Cross Section of Targets: simple targets - sphere, cone-sphere, Transmitter Power, PRF and Range Ambiguities, System Losses (qualitative treatment), Illustrative Problems.

[Text 1: Chapter 2, Chapter 3,Chapter 4]

Module-3	**10 Hours**

MTI and Pulse Doppler Radar:

Introduction, Principle, Doppler Frequency Shift, Simple CW Radar, Sweep to Sweep subtraction and Delay Line Canceler, MI1 Radar with- Power Amplifier Transmitter, Delay Line Cancelers Frequency Response of Single Delay- Line Canceler, Blind Speeds, Clutter Attenuation, MI1 Improvement Factor, N- Pulse Delay-Line Canceler, Digital MTI Processing-Blind phases, I and Q Channels, Digital MTI Doppler signal processor, Moving Target Detector- Original MTD.

[Text 1: Chapter 5, Chapter 6]

Module-4	**10 Hours**

Tracking Radar:

Tracking with Radar- Types of Tracking Radar Systems, Monopulse Tracking- Amplitude Comparison Monopulse (one-and two coordinates), Phase Comparison Monopulse. Sequential Lobing, Conical Scan Tracking, Block Diagram of Conical Scan Tracking Radar, Tracking in Range,Comparison of Trackers.

[Text 1: Chapter 7]

Module-5 **10 Hours**

The Radar Antenna :

Functions of The Radar Antenna, Antenna Parameters, Reflector Antennaa and Electronically Steered Phased array Antennas.

Radar Receiver:

The Radar Receiver, Receiver Noise Figure, Super Heterodyne Receiver, Duplexers and Receivers Protectors, Radar Displays.

[Text 1: Chapter 8, Chapter 9]

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1:. Describe the radar fundamentals.(PO:1,2,3 PSO:1,2)

CO2: . Analyze the radar signals. (PO:1,2,3 PSO:1,2)

CO3:. Explain the working principle of pulse Doppler radars, their applications and limitations. (PO:1,2,3 PSO:1,2)

CO4:. Describe the working of various radar transmitters and receivers. (PO:1,2,3 PSO:1,2)

CO5:.Analyze the range parameters of pulse radar system which affect the system performance. (PO:1,2,3 PSO:1,2)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)

-

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text book:

1. Introduction to Radar Systems- Merrill Skolink, 3e,TMH, 2001

Reference books:

1.Radar Principles, Technology, Applications-ByronEdde, Pearson Education, 2004.

2 Radar Principles-Peebles .Jr, P.Z. Wiley.New York, 1998.

3. Principles of Modem Radar: Basic Principles-Mark A. Rkhards, James A. Scheer,William.A. Holm.Yesdee, 2013

Web links and Video Lectures(e-Resources):

· https://archive.org/details/Skolnik_Radar_Systems_3rd_Ed

· https://ocw.mit.edu/courses/aeronautics-and-astronautics/16-680-radar-systems-engineering-fall-2005/

· https://nptel.ac.in/courses/108/105/108105185/

· https://www.scribd.com/document/393039033/Radar-Engineering-Notes

· https://www.youtube.com/playlist?list=PLbMVogVj5nJS4iIeIiiPao2LrUbwQ8BWs

· https://www.youtube.com/watch?v=YS7-3BvjnIw

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Role Play
- Flipped classroom
- Assessment Methods for 25 Marks (opt two Learning Activities)

- Case Study
- Programming Assignment
- Gate Based Aptitude Test

ENVIRONMENTAL STUDIES AND E WASTE MANAGEMENT (ECE, CIVIL AND MECHANICAL BRANCH ONLY)			
Course Code	**24ES57**	**CIE Marks**	100
Teaching Hours/Week (L: T: P)	1:0:0:0	**SEE Marks**	-
Credits	-	**Total Marks**	100
Contact Hours	14	**Exam Hours**	-
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on:

- Understanding of Ecosystems and Sustainability
- Awareness of Environmental Issues
- Familiarity with Environmental Legislation
- Basic Scientific Principles
- Knowledge of E-waste Lifecycle
- Familiarity with E-waste Recycling Methods
- Awareness of Environmental Policies

Course objectives:

- Identify the major challenges of environmental issues
- Develop skills, critical thinking and demonstrate socio-economic skills for Environmental protection
- Analyze the impact of issues w. r. t. waste management

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) need not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes Critical thinking.
5. Adopt Case study Based Learning (CBL), which fosters students' analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.

Module-1	**2 hrs**
Ecosystem and Sustainability Ecosystems (Structure and Function): Forest, Desert, Wetlands, River, Oceanic and Lake. Sustainability: 17 SDGs-History, targets, implementation, Capacity Development **Text Book 1**: Chapter- 3, e-resource:1	
Module-2	**2hrs**
Natural resources and Energy Advances in Energy Systems (Merits, Demerits, Global Status and Applications): Hydrogen, Solar, OTEC, Tidal and Wind. Natural Resource Management (Concept and case-studies): Disaster Management, Sustainable Mining - case studies and Carbon Trading **Textbook 1**: Chapter- 2	
Module-3	**3 hrs**
Environmental Pollution and Waste Management Environmental Pollution (Sources, Impacts, Corrective and Preventive measures, Relevant Environmental Acts, Case-studies): Surface and Ground Water Pollution; Noise pollution; Soil Pollution and Air Pollution. Waste Management: Bio-medical Wastes; Solid waste; Hazardous wastes; E-wastes; Industrial and Municipal Sludge **Textbook 1:** Chapter- 5	
Module-4	**3 hrs**
Global Environmental Issues Global Environmental Concerns (Concept, policies and case-studies): Ground water depletion/recharging, Climate Change; Acid Rain; Ozone Depletion; Radon and Fluoride problem in drinking water; Resettlement and rehabilitation of people, Environmental Toxicology. **Textbook 1**: Chapter - 6, e-resource:2	
Module-5	4 hrs
Environmental Legislation Environmental Legislation : Water Act 1974, Air Act 1981, Environmental Protection Act 1984, Solid Waste Management Rules-2016, E- Waste management Rule - 2022, Biomedical Waste management-2016. **Textbook 1:** Chapter-6, Textbook 2: Chapter -2, e-resource:3	

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

CO1: Comprehend the principles of ecology and environmental issues pertaining to air, land, and water on a global scale. (PO – 1,2,3,4,6,7 PSO – 1,2)

CO2: Acquire observation skills for solving problems related to the environment. (PO – 1,2,3,4,6,7 PSO – 1,2)

CO3: Conduct survey to describe the realities of waste management system. (PO – 1,2,3,4,5,6,7 PSO – 1,2)

CO4: Apply their ecological knowledge to illustrate and graph a problem and describe the realities that managers face when dealing with complex issues (PO – 1,2,3,4,5,6,7 PSO – 1,2)

CO5: Understand the sources, types, and composition of electronic waste and its impact on the environment and human health. (PO – 1,2,3,4,5,6,7 PSO – 1,2)

Assessment Details

The weightage of Continuous Internal Evaluation (CIE) is 100% and the minimum passing mark for the CIE is 40% of the maximum marks (40 marks out of 100). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the CIE (Continuous Internal Evaluation).

Continuous Internal Evaluation:

- There are 50 marks for the CIE's Assignment component and 50 for the Internal Assessment Test component.
- Each test shall be conducted for 50 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 50 marks
- Any two assignment , if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. The final CIE marks of the course out of 100 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Suggested Learning Resources:

Text Book:

1. S M Prakash , “Environmental Studies” 3rd Edition, Elite Publishing House, Mangalore, 2018.
2. Hester R.E., and Harrison R.M, Electronic Waste Management. Science, 2009.

Reference Books

1. Earch Barucha, “Environmental Studies for UG students”, 2004.
2. Benny Joseph (2005), “Environmental Studies” , Tata McGraw – Hill Publishing Company Limited.
3. R. Rajagopalan, “Environmental Studies- From Crisis to Cure” , 2nd Edition, Oxford university press, New Delhi, 2013.

- https://www.youtube.com/watch?v=VYVriv2vWxE
- https://www.youtube.com/watch?v=yxA6ilJp5fk
- https://www.youtube.com/watch?v=Ccu_wQqT1kA
- https://www.youtube.com/watch?v=hqq4waDUrnk
- https://www.youtube.com/watch?v=RQSM4Z-hgUo
- https://www.youtube.com/watch?v=oepriQ_TOLo
- https://www.youtube.com/watch?v=qS8mfAX1tAk
- NPTEL materials

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning(But are not limited to)

- Field Visits
- Quiz/Assignments/Open book test to develop skills
- Encourage collaborative learning in the class
- Demonstration of Geological models and animations
- Hands on experiments with Rock and Minerals

VLSI Design and Testing			
Course Code	24EC61	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	3:0:0	**SEE Marks**	50
Credits	03	**Total Marks**	100
Contact Hours	40	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Engineering mathematics (calculus, differential equations) and circuit analysis including AC/DC network theorems and frequency response.
- Understanding of electronic devices such as diodes, BJTs, and MOSFETs, including biasing and small-signal models.
- Fundamentals of digital electronics including Boolean algebra, logic gates, combinational and sequential circuits.

Course Objectives:

- This course deals with analysis and design of digital CMOS integrated circuits.
- The course emphasizes on basic theory of digital circuits, design principles and techniques for digital design blocks implemented in CMOS technology.
- This course will also cover switching characteristics of digital circuits along with delay and power estimation.
- Understanding the CMOS sequential circuits and memory design concepts.
- Explore the knowledge of VLSI Design flow and Testing

Teaching-Learning Process (General Instructions)

Teachers can use the following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Demonstration based Teaching

Module-1	**8 Hours**

Introduction to CMOS Circuits: Introduction, MOS Transistors, MOS Transistor switches, CMOS Logic, Alternate Circuit representation, CMOS-nMOS comparison.
[Text 1: 1.1,1.2,1.3,1.4,1.5.1.6.]

Module-2	**8 Hours**

MOS Transistor Theory: n-MOS enhancement transistor, p-MOS transistor, Threshold Voltage, Threshold voltage adjustment, Body effect, MOS device design equations, V-I characteristics, CMOS inverter DC characteristics, Influence of βn / βp ratio on transfer characteristics, Noise margin, Alternate CMOS inverters. Transmission gate DC characteristics. Latch-up in CMOS.
[Text 1: 2.1,2.2,2.3,2.4,2.5.2.6.]

Module-3	8 Hours
CMOS Process Technology: Silicon Semiconductor Technology, CMOS Technologies, Layout Design Rules. [Text 1: 3.1,3.2,3.3.] **Circuit Characterization and Performance Estimation:** Introduction, Resistance Estimation, Capacitance Estimation, Switching Characteristics, CMOS gate transistor sizing, Determination of conductor size, Power consumption, Charge sharing, Scaling of MOS transistor sizing, Yield. [Text 1: 4.1,4.2,4.3,4.4,4.5.4.6.4.7,4.8,4.9,4.10]	
Module-4	**8 Hours**
CMOS Circuit and Logic Design: Introduction, CMOS Logic structures, CMOS Complementary logic, Pseudo n-MOS logic, Dynamic CMOS logic, Clocked CMOS Logic, Cascade Voltage Switch logic, Pass transistor Logic, Electrical and Physical design of Logic gates, The inverter, NAND and NOR gates, Body effect, Physical Layout of Logic gates, Input output Pads. [Text 1: 5.1,5.2,5.2.1, , 5.2.2, 5.2.3, 5.2.4, 5.2.6, 5.2.8, 5.3,5.3.1,5.3.2, 5.3.4 ,5.3.8,5.5]	
Module-5	**8 Hours**
Sequential MOS Logic Circuits: Introduction, Behaviour of Bistable Elements (Excluding Mathematical analysis) SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, Clocked SR Latch, Clocked JK Latch [Text 2: 8.1, 8.2, 8.3, 8.4] **Structured Design and Testing:** Introduction, Design Styles, Testing [Text 1: 6.1, 6.2. 6.5] **Introduction to ASIC:** Types of ASIC and ASIC Design flow [Text 3:1.1,1.2,1.3]	

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Apply the fundamentals of semiconductor physics in MOS transistors and analyze the geometrical effects of MOS transistors. (PO – 1,2,3,4,5,11 PSO – 1,2,3)

CO2: Design and realize combinational, sequential digital circuits and memory cells in CMOS logic.(PO – 1,2,3,4,5,11 PSO – 1,2,3)

CO3: Analyze the synchronous timing metrics for sequential designs and structured design basics. (PO – 1,2,3,4,5,11 PSO – 1,2,3)

CO4: Understand designing digital blocks with design constraints such as propagation delay and dynamic power dissipation. (PO – 1,2,3,4,5,11 PSO – 1,2,3)

CO5: Understand the concepts of Sequential circuits design and VLSI testing (PO – 1,2,3,4,5,11 PSO – 1,2,3)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the regulations; if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

The Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books:

1. Principals of CMOS VLSI Design A System approach Neil H E Weste and Kamran Eshraghain . Addition Wisley Publishing company.

2. "CMOS Digital Integrated Circuits: Analysis and Design", Sung Mo Kang & Yosuf Leblebici, Third Edition, Tata McGraw-Hill.

3. Michael John Sebastian Smith, "Application Specific Integrated Circuits", Addison-Wesley Professional-ISBN-13**:** 978-0-201-50022-6, 2008

Reference Books:

1. "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, and David Money Harris 4th Edition, Pearson Education.

2. "Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005.

Web links and Video Lectures(e-Resources):

- https://www.classcentral.com/course/youtube-digital-vlsi-testing-47862
- https://www.classcentral.com/course/youtube-electronics-advanced-vlsi-design-47530
- https://www.classcentral.com/course/youtube-overview-of-vlsi-design-flow-i-437246
- https://www.classcentral.com/course/youtube-overview-of-vlsi-design-flow-iv-437249
- https://www.nptelprep.in/courses/117103125/materials
- https://archive.nptel.ac.in/courses/106/103/106103116/
- https://www.nptelprep.in/courses/106103016/
- https://www.classcentral.com/course/youtube-overview-of-vlsi-design-flow-i-437246
- https://www.youtube.com/watch?v=YpbtAwmYCcI
- https://www.youtube.com/watch?v=Em0qaYBmQ3o
- https://www.youtube.com/watch?v=QygaA9tJa7g

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning(But are not limited to)

- Role Play
- Flipped classroom
- Assessment Methods for 25 Marks (opt two Learning Activities)
    - Case Study
    - Assignment & online certifications
    - **o** Simulation of circuits using suitable software

Embedded System Design			
Course Code	24EC61(IPCC)	**CIE Marks**	50
Teaching Hours/Week (L: T:P)	3:0:2	**SEE Marks**	50
Credits	04	**Total Marks**	100
Contact Hours	40 hours Theory + 10 Lab slots	**Exam Hours**	03
Examination type (SEE)	Theory		

Prerequisites:

Students should have a basic understanding of:

- Microprocessors
- Microcontrollers

Course Objectives:

- Identify the key components of an embedded system, understand their functions, and select appropriate components based on application requirements.
- Understand the programming of embedded peripherals using Embedded C.
- Comprehend the fundamentals of ARM-based systems, including architecture, register organization, stack operation, Memory Protection Unit (MPU), debug interfaces, and interrupt handling mechanisms.
- Understand the ARM Instruction Set Architecture (ISA) and its application in embedded system development.
- Understand the concepts of Real-Time Operating Systems (RTOS), Integrated Development Environments (IDE), and the architectural features of STM32 microcontrollers, including pin configuration and peripheral mapping.

Teaching-Learning Process (General Instructions)

The following are sample strategies that teachers may adopt to enhance the attainment of various Course Outcomes (COs):

1. In addition to the traditional lecture method, innovative teaching approaches may be adopted to strengthen student's theoretical understanding and practical application skills.
2. Provide real-world examples to improve conceptual clarity and application-oriented learning.
3. Encourage and guide students towards effective self-study practices.
4. Assign homework, quizzes, and graded assignments regularly, while monitoring and documenting student's academic progress.
5. Promote group learning activities to enhance students' creativity, teamwork, and analytical abilities.
6. Use short subject-related video lectures in the following ways:
   - As an introduction to new topics (pre-lecture activity).
   - As a revision tool for completed topics (post-lecture activity).
   - As supplementary examples for better understanding (post-lecture activity).
   - As additional support material for difficult topics (pre- and post-lecture activity).
   - As model solutions for selected exercises and problems (post-lecture activity).

Module-1	**08 Hours**

Introduction to Embedded System:

Introduction to Embedded Systems: Definition of Embedded Systems, Embedded Systems vs. General Computing Systems, History and Evolution of Embedded Systems, Classification of Embedded Systems, Major Application Areas, and Purpose of Embedded Systems. Overview of Typical Embedded Systems: Comparison of Microprocessors and Microcontrollers, RISC vs. CISC Architecture, Harvard vs. Von Neumann Architecture, and Big-endian vs. Little-endian Processors.Memory and Interfacing Components: Types of ROM and RAM, Sensors and Actuators, and the I/O Subsystem including I/O Devices such as LEDs, 7-Segment Displays, Optocouplers, Relays, Piezo Buzzers, and Push Button Switches. Communication and Firmware: On-board and External Communication Interfaces, Embedded Firmware, and Other Essential System Components.

Text book 1: Chapter 1,2

Module-2	**08 Hours**

Embedded System Design Concepts:

Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modeling (excluding UML), Embedded firmware design and development (excluding C language).

Text book 1: Chapter-3,4 (4.1, 4.2.1 and 4.2.2 only), Chapter-7 (7.1, 7.2 only), Chapter-9 (9.1, 9.2, 9.3.1, 9.3.2 only)

Module-3 **08 Hours**

ARM Embedded Systems: Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications. ARM Processor Fundamentals, ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions.

Text book 2: Chapter 1, 2

Module-4 **08 Hours**

Introduction to the ARM Instruction set: Introduction, Data processing instructions, Load – Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, ARMv5E extensions, Conditional Execution.

Text book 2: Chapter 3

Module-5 **08 Hours**

RTOS and IDE, STM32 Microcontrollers Architecture and Ecosystem:

How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil).

STM Microcontrollers Series- Introduction, Components of STM32F407VG, Pin configuration of STM32F407VG, Industrial applications of STM32F407VG, Emerging trends in embedded systems, New applications in embedded systems, Careers and opportunities in embedded systems.

Text book 1: Chapter-10.10, Chapter-12, Chapter-13 (only 13.1), and **Text 3:** Chapter 13, 25.

PRACTICAL COMPONENT OF IPCC

Conduct the following experiments on an ARM CORTEX M3 evaluation board to learn Assembly Language Program and using evaluation version of Embedded 'C' & Keil uVision-4 tool/compiler.

Sl.NO	Experiments
1.	Write a program to find the sum of the first 10 integer numbers.
2.	Write an Assembly Language Program (ALP) to i) Multiply two 16-bit numbers. ii) Add two 32-bit numbers.
3.	Write a program to find the factorial of a number
4.	Write a program to add an array of 16 bit numbers and store the 32 bit result in internal RAM.
5.	Write a program to find the square of a number (1 to 10) using a look-up table.
6.	Write a program to find the largest or smallest number in an array of 32 numbers.
7.	Write a program to arrange a series of 32 bit numbers in ascending/descending order.
8.	Write a program to count the number of ones and zeros in two consecutive memory locations.
9.	Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.
10.	Interface a DAC and generate Triangular and Square waveforms.
11.	Display the Hex digits 0 to F on a 7-segment LED interface, with a suitable delay in between.
12.	Interface a simple Switch and display its status through Relay, Buzzer and LED

Course outcomes(Course Skill Set):

At the end of the course, the student will be able to:

CO1: Illustrate the basic hardware components of embedded systems and select appropriate components based on system characteristics and performance requirements. (PO-1,2 PSO-1,2)

CO2: Analyze hardware–software co-design principles and apply firmware design methodologies in embedded system development. (PO-1,2 PSO-1,2)

CO3: Outline the architectural features, memory organization, and instruction set of the 32-bit ARM Cortex-M3 microcontroller. (PO-1,5 PSO-1,2)

CO4: Develop and implement embedded applications using ARM Cortex-M3 by applying programming concepts, peripheral interfacing, and debugging techniques. (PO-1,2,5,9,10 PSO-1,2,3)

CO5: Identify the need for a Real-Time Operating System (RTOS), Integrated Development Environment (IDE), and architectural features of STM32 microcontrollers in embedded applications. (PO-1,2,5,11 PSO-1,2)

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)

- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are 25 marks and that for the practical component is 25 marks.
- 25 marks for the theory component are split into 15 marks for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and 10 marks for other assessment methods. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for 25 marks).
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- 15 marks for the conduction of the experiment and preparation of laboratory record, and 10 marks for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments, write-ups are added and scaled down to 15 marks.
- The laboratory test (duration 02/03 hours) after completion of all the experiments shall be conducted for 50 marks and scaled down to 10 marks.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for 25 marks.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC

SEE for IPCC Theory

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

Suggested Learning Resources:

Textbook:

1. Shibu K V, "**Introduction to Embedded Systems",** Tata McGraw Hill Education
2. Andrew N Sloss, Dominic System and Chris Wright, **"ARM System Developers Guide"**, Elsevier, Morgan Kaufman publisher, 1st Edition, 2008.
3. Sadia Adrees & Sheik Muhammadi Ibraeem, **"Embedded Systems for Engineers & Students",** Kindle 2nd Edition, March 04, 2024.

Reference Books

1. Peckol, **"Embedded system Design",** John Wiley and Sons,2010
2. Steve Furber, **"ARM System-on-Chip Architecture"**, 2nd Edition, Pearson Education

Web links and Video Lectures(e-Resources):

1.https://archive.nptel.ac.in/courses/106/105/106105193/

2.https://onlinecourses-archive.nptel.ac.in/noc18_cs05/course?utm_source=chatgpt.com

3.https://developer.arm.com/documentation/dui0068/b/ARM-Instruction-Reference

4.https://www.udemy.com/course/introduction-to-arm-cortex-m3-and-m4-processors/

5.https://www.nptel.ac.in/courses/106105193?utm_source=chatgpt.com

6.www.Nuvoton .com/websites on Advanced ARM Cortex Processors

7. https://alison.com/tag/embedded-systems

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning (But are not limited to)

- Flipped classroom sessions for selected topics.
- Technical seminars on recent trends and applications in Embedded Systems.
- Mini projects based on ARM/STM32 microcontrollers and embedded applications.
- Completion of relevant MOOC/NPTEL certification courses.
- Programming assignments related to Embedded C and ARM programming.
- Conducting quizzes to strengthen conceptual understanding and problem-solving skills.
- Hands-on experiments involving interfacing of sensors, actuators, and communication peripherals.
- Group discussions and collaborative learning activities on embedded system design challenges.

VLSI Design and Testing Laboratory			
Course Code	24ECL63	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	0:0:2	**SEE Marks**	50
Credits	01	**Total Marks**	100
Contact Hours	12 Lab slots	**Exam Hours**	3
Examination type (SEE)	Practical		

Prerequisites:

The students should have knowledge on

- Digital Electronics and Electronic Devices, including MOSFET operation and combinational/sequential circuits.
- CMOS logic fundamentals and timing concepts
- Basic understanding of Verilog and simulation tools

Course Objectives:

This laboratory course enables students to

- Design, model, simulate and verify digital circuits.
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist.
- Perform RTL-GDSII flow and understand the ASIC Design flow.

Teaching-Learning Process (General Instructions)

Teachers can use the following strategies to accelerate the attainment of the various course outcomes.

1. Collaborative Learning
2. Demonstration based Teaching
3. Use of Simulation Tools
4. Conceptual Linking

Sl. No	Experiments
1	Design a 4-Bit Adder • Write a Verilog description • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and generate the gate level netlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required.
2	4-Bit Shift and add Multiplier • Write Verilog Code • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the gate level netlist.

	From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required
3	32-Bit ALU Supporting 4-Logical and 4-Arithmetic operations, using case and if statement for ALU Behavioral Modeling • Write Verilog description • Verify functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist • Identify Critical path
4	Flip-Flops (D,SR and JK) • Write the Verilog description • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the gate level netlist. From the report gate level netlist identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required. • Verify the functionality using Gate level netlist and compare the results at RTL and gate level netlist.
5	Four bit Synchronous MOD-N counter with Asynchronous reset • Write Verilog Code • Verify functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist Identify Critical path • Verify the functionality using Gate level netlist and compare the results at RTL and gate level netlist.
6	a) Construct the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following: i. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and the time period of 20ns and plot the input voltage and output voltage of designed inverter? ii. From the simulation result compute tpHL, tpLH and td for all three geometrical settings of width? iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter. b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre layout simulations and compare the results.
7	Capture the schematic of 2-input CMOS NOR gate having similar delay as that of CMOS inverter computed in experiment above. Verify the functionality of NOR gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.
8	Construct the schematic of the Boolean Expression Y= $\overline{AB + CD + E}$ using CMOS Logic. Verify the functionality of the expression find out the delay td for some combination of input vectors. Tabulate the results.
9	a) Construct the schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measure the Unit Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB.

	b) Draw Layout of common source amplifier, use optimum layout methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, compare the results with prelayout simulations. Record the observations.
10	a) Construct the schematic of two-stage operational amplifier and measure the following: i. Unity gain Bandwidth ii. dB Bandwidth iii. Gain Margin and phase margin with and without coupling capacitance iv. Use the op-amp in the inverting and non-inverting configuration and verify its functionality. v. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations. b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in part a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations and perform the comparative analysis.
	Demonstration Experiments
1	UART • Write Verilog description • Verify the Functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist, Identify Critical path
2	Design and characterize 6T binary SRAM cell and measure the following: • Read Time, Write Time, SNM, Power • Draw Layout of 6T SRAM, use optimum layout methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Design and simulate combinational and sequential digital circuits using Verilog HDL. (PO-1,2,3,4,9,10,PSO-1,2,3)

CO2: Understand the synthesis process of digital circuits using the EDA tool. (PO-1,2,3,4,9,10,PSO-1,2,3)

CO3: Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist. (PO-1,2,3,4,9,10,PSO-1,2,3)

CO4: Design and simulate basic CMOS circuits like inverter, NOR gate and any Boolean Expression. (PO-1,2,3,4,9,10,PSO-1,2,3)

CO5: Perform RTL_GDSII flow and understand the stages in ASIC design. (PO-1,2,3,4,9,10,PSO-1,2,3)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50

marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are 50 Marks. The split-up of CIE marks for record/ journal and test are in the ratio 60:40.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- The department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva- voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to 20 marks (40% of the maximum marks).
- The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course are 50 Marks.

1. SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute.
2. The examination schedule and names of examiners are informed to the university before the

   Conduction of the examination.
3. These practical examinations are to be conducted between the schedules mentioned in the academic calendar of the University. All laboratory experiments are to be included for practical examination.
4. (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.
5. Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.

6. Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners
7. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners) Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.
8. The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. Verilog HDL: A Guide to Digital Design and Synthesis, Samir Palnitkar, 2nd Edition, 2003, Prentice Hall PTR (Pearson Education).
2. SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling, Stuart Sutherland, Simon Davidmann and Peter Flake, 2nd Edition, 2006, Springer Science+Business Media.
3. FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version, Pong P. Chu, 1st Edition, 2008, Wiley-Interscience (John Wiley & Sons, Ltd.).

Web links and Video Lectures(e-Resources):

- https://www.nptelprep.in/courses/106103016/materials
- https://vlsiresources.com/frontendvlsi/
- http://vlsi-iitg.vlabs.ac.in/
- https://www.edaplayground.com/
- https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice.html
- https://www.youtube.com/watch?v=J4gTC-KFLi8&list=PL4isOTp6hCIdNn_cFSPCDhoSrTvj5m8CE

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning(But are not limited to)

- Troubleshooting sessions
- Simulation based activities

VLSI Physical Design			
Course Code	24EC64A	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	4:0:0	**SEE Marks**	50
Credits	04	**Total Marks**	100
Contact Hours	50	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on:

- Digital Electronics & Logic Design
- CMOS VLSI Design & Semiconductor Devices
- Data Structures & Algorithms
- Hardware Description Languages (HDL)

Course Objectives:

Understand the complete RTL-to-GDSII physical design pipeline, including the functional role of industry-standard file formats like LEF, DEF, SDC, and Liberty.

Analyze and apply core mathematical algorithms used for graph partitioning, floorplanning, standard-cell placement, and global/detailed routing.

Develop robust power distribution grids to minimize IR drop and construct optimized clock trees to eliminate skew and latency variations.

Perform Static Timing Analysis (STA) to identify and fix setup, hold, and signal integrity (crosstalk) violations across multiple operating conditions.

Validate layouts against manufacturing constraints using Design Rule Checking (DRC) and Layout Versus Schematic (LVS) verification tools.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of combinational and sequential circuits
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.

- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.
- Give Programming Assignments.

Module-1	10 Hours

Introduction to Physical Design Flow & CMOS Basics

ASIC/FPGA design cycles, RTL-to-GDSII backend design stages, introduction to standard input/output design formats (LEF, DEF, SDC, Liberty .lib CMOS fundamentals, layout design rules, and stick diagrams.

Text 1: 1.1,1.2,1.3,2.1,2.2
Text2: 1.1,1.2,1.3
Text3:1.1,1.2,2.1,2.4
Reference 1:1.4,1.5

Module-2	10 Hours

Partitioning, Floorplanning, and Power Planning

System-level partitioning (Kernighan-Lin, Fiduccia-Mattheyses algorithms), core budgeting, block sizing, aspect ratio optimization [2], macro placement, pin assignment [2], power grid planning (rings, straps, rails), and IR drop analysis.

Text1:2.3 ,2.4,2.5,3.1,3.2,3.3,3.5
Text2: 2.1,2.2,2.3,2.4
Text3:5.2,5.3,6.1,6.3

Module-3	10 Hours

Placement and Clock Tree Synthesis (CTS)

Global placement, detailed placement, congestion minimization, wirelength optimization, clock planning, skew and insertion delay minimization, clock buffer tree structures (H-Tree, Fishbone), and multi-corner multi-mode (MCMM) timing grids.

Text 1: 4.1,4.2,4.4,6.1,6.2,6.3
Text 2: 3.1,3.2,4.1,4.3
Text 3:7.2,9.1,9.2

Module-4	**10** Hours

Module 4: Global and Detailed Routing

Coarse-grain routing, grid and track assignments, maze routing (Lee's algorithm), line-probe algorithms, channel routing [2], signal integrity challenges, crosstalk reduction, and via optimization.

Text 1: 5.1,5.2,5.4,5.5

Text 2:5.1,5.2,5.4
Text 3:8.1,8.2,10.1,10.2

Module-5 10 Hours

Static Timing Analysis (STA), Sign-off, and Testing

Setup and hold time constraints, timing violation closure, Design Rule Checks (DRC), Layout Versus Schematic (LVS), Design for Testability (DFT), scan insertion, and Engineering Change Orders (ECO).

Text 1: 7.1,7.2,7.3,7.5
Text 2: 6.1,6.2,7.1,7.2
Text 3: 12.1,14.1

Course outcomes (Course Skill Set):
At the end of the course, the student will be able to:
CO1: Analyze the standard semiconductor ASIC backend design flow, translating RTL netlists and design constraints (LEF, DEF, SDC, Liberty) into a structured physical layout environment.

(PO-1,3 PSO-1,2)

CO2: Apply architectural partitioning, floorplanning, and power planning techniques to minimize core congestion and control IR drop across the chip grid.

(PO-1,2,3,5 PSO-1,2)

CO3: Evaluate placement strategies and Clock Tree Synthesis (CTS) configurations to optimize cell density while minimizing clock skew and insertion delays.

(PO-1,2,3,4,5 PSO-1,2)

CO4: Synthesize optimal global and detailed routing pathways using network flow and maze routing algorithms while mitigating signal crosstalk.

(PO-1,2,3,4,5 PSO-1,2)

CO5: Perform Static Timing Analysis (STA) and physical sign-off verification

DRC/LVS) to validate chip layout compliance against strict tape-out rules.

(PO-1,2,3,4,5 PSO-1,2)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.

- Any two assignment methods, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks).
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:
Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours).
1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with 3. a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:
Text Books

1.VLSI Physical Design: From Graph Partitioning to Timing Closure – Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu (Springer).
2.Physical Design Essentials: An ASIC Design Implementation Perspective – Khosrow Golshan (Springer).
3.Algorithms for VLSI Physical Design Automation – Naveed A. Sherwani (Springer/Kluwer).

Reference Books:
1.CMOS VLSI Design: A Circuits and Systems Perspective – Neil Weste, David Harris (Pearson).
2.Application-Specific Integrated Circuits – Michael John Sebastian Smith (Addison-Wesley)

Web links and Video Lectures(e-Resources):

- https://www.youtube.com/playlist?list=PLCmoXVuSEVHlEJi3SwdyJ4EICffuyqpjk
- https://www.youtube.com/watch?v=_sNDVdRYYbI&t=16
- https://www.youtube.com/playlist?list=PLFXvEi07abL0Mzx1a9Gz588Vy3do0AOZC

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Flipped classroom
- Assessment Methods for 25 Marks (opt two Learning Activities)
  - Programming Assignment
  - Group Discussion/Quiz.

- Demonstration of Verilog and FPGA concepts.
- Case Study on small design and implementation on FPGA's.

Digital Image Processing			
Course Code	24EC64B	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	(3:2:0)	**SEE Marks**	50
Credits	4	**Total Marks**	100
Contact Hours	40	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on:

Linear algebra (matrices/vectors), calculus, probability/statistics, and discrete signal processing (Fourier transforms, convolution).

Course Objectives:

- Understand the fundamentals of digital image processing.
- Apply spatial domain enhancement techniques.
- Analyze image transforms in frequency domain.
- Understand color image processing techniques.
- Design basic image restoration techniques.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Show Video/animation films to explain the functioning of various image processing concepts
2. Encourage cooperative (Group) Learning through puzzles, diagrams, coding etc., in the class.
3. Encourage students to ask questions and investigate their own ideas helps improve their problem-solving skills as well as gain a deeper understanding of academic concepts.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Students are encouraged to do coding based projects to gain knowledge in image processing.
6. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
7. Topics will be introduced in multiple representations.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding
9. Arrange visits to nearby PSUs such as CAIR (DRDO), NAL, BEL, ISRO, etc., and small-scale software industries to give industry exposure.

Module-1 **10 Hours**

Digital Image Fundamentals: What is Digital Image Processing? Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels.

Text book 1: Chapter 1, Chapter 2: Sections 2.1 to 2.5]

Module-2 **10 Hours**

Spatial Domain: Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters

Text book 1: Chapter 3: Sections 3.2 to 3.6

Module-3 **10 Hours**

Image Transforms :

Introduction,need for transform,Image transforms,2D-DFT, Properties of 2D-DFT,Walsh Transform, Hadamard Transform

Self Study: DCT and Haar Transform

Text book 2: Chapter 4: Sections 4.1,4.2,4.3,4.5,4.6,4.8,4.9

Module-4 **10 Hours**

Frequency Domain: Basics of Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters. Color Image Processing: Color Fundamentals, Color Models, Pseudo-color Image Processing.

Text book 1: Chapter 4: Sections 4.7 to 4.9 and Chapter 6: Sections 6.1 to 6.3

Module-5 **10 Hours**

Restoration: A model of the Image Degradation/Restoration Process, Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering.

Text book 1: Chapter 5: Sections 5.1, to 5.4.3, 5.7, 5.8

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Explain fundamentals of digital image formation and sampling.(PO-1,2 PSO-1,2)

CO2: Apply spatial enhancement techniques.(PO-1,2 PSO-1,2,3)

CO3: Analyze and compute frequency domain transforms.(PO-1,2 PSO-1,2,3)

CO4: Implement color image processing methods.(PO-1,2 PSO-1,2,3)

CO5: Design basic image restoration techniques.(PO-1,2 PSO-1,2,3)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)

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Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text book:

1. Digital Image Processing- Rafael C Gonzalez & Richard E Woods,3rd Edition
2. Digital Image Processing-S.Jayaraman,S.Esakkirajan,T.Veerakumar-Tata McGraw Hill,3rd Reprint, 2010

Reference book:

1. Fundamentals of Digital Image Processing- A K Jain, PHI Learning Private Limited 2014

Web links and Video Lectures(e-Resources):

- Image databases, https://imageprocessingplace.com/root_files_V3/image_databases.htm
- Student support materials, https://imageprocessingplace.com/root_files_V3/students/students.htm
- NPTEL Course, Introduction to Digital Image Processing, https://nptel.ac.in/courses/117105079
- Computer Vision and Image Processing, https://nptel.ac.in/courses/108103174

- Image Processing and Computer Vision – Matlab and Simulink,
- https://in.mathworks.com/solutions/image-video-processing.htm

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning(But are not limited to)

- Role Play
- Flipped classroom
- Case Study
- Programming Assignment
- Gate Based Aptitude Test

Real Time Operating System			
Course Code	24EC64C	**CIE Marks**	50
Teaching Hours/Week (L: T:P)	4:0:0	**SEE Marks**	50
Credits	4	**Total Marks**	100
Contact Hours	50	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

- The students should have knowledge on microprocessor and microcontroller

Course Objectives:

- To understand the basics of Real time operating Systems (RTOS).
- To understand the working of real-time operating systems and real- time databases.
- To analyze the Kermel object concept
- To analyze the memory management concept
- To analyze embedded software development process

Teachers can use the following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Hands on activity Teaching

Module-1 **10 Hours**

UNIT I: Real life examples of Embedded system, Real time systems,Basics of Developing for Embedded systemOverview of linker and linking process,Executable and linking format ,mapping of image into targeting system Embedded system Initialization.(Only concept no programming)

Text book 1: Chapter 1.1,1.2,2.1,2.2,2.4,2.4.3.2,3.3,3.4

Module-2 **10 Hours**

UNIT II: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, Tasks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Thread Safe Re-entrant Functions.

Text book 1:Chapter 4.2,4.3,4.4,4.5,4.6,4.7,5,.2,5.3,5.6

Module-3 **10 Hours**

Other Kernel Objects: Pipes, Event Registers, Signals, Condition Variables, Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem, Port-mapped v/s Memory mapped I/O

and DMA, Exceptions and Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers,

Text book 1: Chapter 8.1,8.2,8.3,8.5,9.2,9.3,12.1,12.2,12.3

Module-4 **10 Hours**

Memory management, Dynamic Memory Allocation in Embedded Systems, Fixed size memory management in Embedded systems, Blocking v/s Non-blocking memory functions, Synchronizations and Communications, Resource Classification, Deadlocks Detection and Recovery, Priority Inversions.

Text book 1: Chapter 13.1,13.2,13.3,13.5,16.2,16.3,16.4

Module-5 **10 Hours**

Basic function and types of RTOS**,** RT Linux, Micro C/OS-II, Vx Works, Introduction to embedded software development process and tool , host and Target machine, Embedded Linux, Tiny OS, and Basic Concepts of Android OS(Only architecture).

Text book 2: Chapter 9.1,9.2,9.3,13.1,13.2,13.3,13.4,13.5

Suggested Learning Resources:

Text Books

1. Real Time Concepts for Embedded Systems,Qing Li Publisher: ElsevierEdition: 2011

2. Embedded Systems- Architecture, Programming and Design, Rajkamal,Publisher: TMH Edition: second

Reference Book

1. Advanced UNIX Programming, W. Richard Stevens Addison-Wesley Professional **Edition:** 3rd Edition (Originally published in 1992)

2. Embedded Linux: Hardware, Software and Interfacing, Dr. Craig Hollabaugh PuAddison-Wesley Professional,Edition: 2002

Course outcomes(CourseSkillSet):

At the end of the course,the student will be able to:

CO1 To understand the basics of Real time operating Systems (RTOS)(PO-1,2 PSO –1)

CO2 To develop real-time algorithms for task scheduling. **:**(PO–1,2 PSO –1)

CO3 To understand the working of real-time operating systems and real- time database.(PO–1,2 PSO –1,2)

CO4 To work on design and development of protocols related to real-time(PO–1,2,3 PSO –1,2)

Assessment Details (both CIE and SEE):

CIE for the theory component of the IPCC (maximum marks 50)

The Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

CIE for the practical component of the IPCC

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Web links and Video Lectures(e-Resources):

1. https://nptel.ac.in/courses/106105172

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning (but are not limited to)

- Role Play
- Case Study
- Programming Assignment

Optical Communication Networks			
Course Code	24EC64D	**CIE Marks**	50
Teaching Hours/Week(L:T:P:S)	3:0:0:0	**SEE Marks**	50
Total Hours of Pedagogy	40	**Tota l Marks**	100
Credits	03	**Exam Hours**	03 Hours
Examination type (SEE)			

Prerequisites:

Understanding Kepler's laws, satellite orbits (LEO, MEO, GEO), look angles, and orbital perturbations.

- Fundamentals of antennas, frequency bands, and wave propagation.
- Knowledge of the space segment (transponders, attitude, and orbit control systems AOC) and ground segment (earth stations).
- Understanding light propagation, attenuation, dispersion (polarization mode dispersion), and nonlinear effect
- Basic Knowledge of lasers, LEDs, photodetectors, and amplifiers (EDFA).
- Familiarity with WDM (Wavelength Division Multiplexing) systems and intensity modulation.

Course objectives:

- Understand the basic principles of satellite orbits and trajectories
- Study of electronic systems associated with a satellite and the earth station.
- Understandthevarioustechnologiesassociatedwiththecommunicationsatellite.
- Learnthebasicprincipleofopticalfibercommunicationwithdifferentmodesoflightpropagation.
- Understand the transmission characteristics and losses, optical components and its applications in optical communication.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method(L)does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/ animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group)Learning in the class.
4. Askat least three HOTS(Higher-order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL),which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in multiple representations.
7. Showthedifferentwaystosolvethesameproblemandencouragethestudentstocomeup with their own creative ways to solve them.

Discuss how every concept can be applied to the real world-and when that's possible it helps improve the students' understanding.

Module-1	8 Hours

Introduction of Optical Communication: Introduction, general system, advantages, disadvantages and applications of optical fiber communication, optical fiber waveguides, Ray theory, single mode fiber, cutoff wavelength, mode field diameter, group velocity, phase velocity, group delay, Fiber materials, Optical Cables.
[Text1:2.1,2.2,2.3,2.4,2.5,3.3,3.4,3.5,3.6,3.7] L1,L2

Module-2	8 Hours

Transmission Characteristics of Optical Fiber: Transmission Characteristics of Optical Fibers, Attenuation, Absorption, Scattering Losses, Bending Loss, Dispersion, Intra-modal Dispersion, Inter-modal Dispersion.
[Text1:4.1,4.5,4.6,4.7,4.8,8.1,8.2,8.3,8.4,8.5,8.6,8.7]L1,L2

Module-3	8 Hours

Optical sources: Light Emitting diodes: LED Structures, Light SourceMaterials, Quantum Efficiency and LED Power, Modulation. Laser Diodes: Modes and Threshold conditions, Rate equation, External Quantum Efficiency, Resonant Frequencies.

Photodetectors: Physical principles of Photodiodes, Photo detector noise, Detector response time. Networking
[Text2: 4.2,4.3, 6.1, 10.1,10.3, 10.4,10.5, 10.7] L1,L2

Module-4	8 Hours

WDM Concepts and Components: Overview of WDM: Operational Principles ofWDM, WDM standards, Mach-Zehnder Interferometer Multiplexers, Isolators and Circulators, Fiber grating filters, Dielectric Thin-Film Filters, Diffraction Gratings.

Optical amplifiers: Basic application and Types. Semiconductor optical amplifiers, Erbium Doped Fiber Amplifiers, Raman Amplifiers, Wideband Optical Amplifiers.

Module-5	8Hours

Optical networks, Protocols and standards: WDM standards, Optical networks SONET/SDH, SONET rings and architectures, GPON.
Optical devices: EDFA, Directional couplers, Isolators, circulators, Multiplexers, Star couplers. Optical sensors for IOT and smart devices.

Course Outcomes:

At the end of the course, students will be able to:
CO1: Classify and describe working of optical fiber with different modes of signal propagation. Optoelectronics & Fiber(PO-1,2,3 PSO-1,2)
CO2: Describe the transmission characteristics and losses in optical fiber communication. (PO-1,2,3 PSO-1,2)
CO3: Describe the construction and working principle of optical connectors, multiplexers and amplifiers. (PO-1,2,3 PSO-1,2)
CO4: Describe the constructional features and the characteristics of optical Sources and detectors. (PO-1,2,3 PSO-1,2)

CO5: illustrate the networking aspects of optical fiber and describe various standards associated with it. (PO-1,2,3 PSO-1,2)

Assessment Details (Both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam(SEE) is 50%.The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing markis 35% o fthe maximum mark s(18 out of 50 marks). The studentis declared as a pass in thec ourse if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE(Continuous Internal Evaluation) and SEE(Semester End Examination) taken together.

Continuous Internal Evaluation:

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks).
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

The question paper will have ten questions. Each question is set for 20 marks.

There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.

The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books:

1. Gerd Keiser, Optical Fiber Communication, 5th Edition, Mc Graw Hill Education (India) Private Limited, 2015.ISBN:l-25-900687-5.

2 John M Senior, Optical Fiber Communications, Principles and Practice, 3td Edition, Pearson Education, 2010,ISBN:978-81-317-3266

Reference books

1. Fiber optic communication– Joseph C Palais: 4th Edition, Pearson Education.

WeblinksandVideoLectures(e-Resources):

- https://nptel.ac.in/courses/117105131
- BasicIntroductionToSatelliteCommunications|SatelliteCommunications - YouTube
- HowSatelliteWorks(Animation)-YouTube
- Introductionvideo:FiberOpticCommunicationTechnology(youtube.com)

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning:

- Seminar
- Flipped classroom
- Assessment Methods Marks (opt two Learning Activities)
- Quiz
- Assignment

Research Methodology and IPR			
Course Code	24RM66	**CIE Marks**	50
Teaching Hours/Week (L: T:P)	2:2:0	**SEE Marks**	50
Credits	3	**Total Marks**	100
Contact Hours	40	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites: Nil

Course Objectives:

- To Understand the basics of research and its types.
- To Learn the concept of Literature Review, Technical Reading, Attributions and Citations.
- To learn Ethics in Engineering Research
- To discuss Geographical Indicator.

Teaching-Learning Process (General Instructions)

Teachers can use the following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Hands on activity Teaching

Module-1 **8 Hours**

Introduction: Meaning of Research, Objectives of Engineering Research, and Motivation in Engineering Research, Types of Engineering Research, Finding and Solving a Worthwhile Problem. Ethics in Engineering Research, Ethics in Engineering Research Practice, Types of Research Misconduct, Ethical Issues Related to Authors

Text book 1: Chapter-1,2

Module- 2 **8 Hours**

Literature Review and Technical Reading, New and Existing Knowledge, Analysis and Synthesis of Prior Art Bibliographic Databases, Web of Science, Google and Google Scholar, Effective Search: The Way Forward Introduction to Technical Reading Conceptualizing Research, Critical and Creative Reading, Taking Notes While Reading, Reading Mathematics and Algorithms, Reading a Datasheet. Attributions and Citations: Giving Credit Wherever Due, Citations: Functions and Attributes, Impact of Title and Keywords on Citations, Knowledge Flow through Citation, Citing Datasets, Styles for Citations, Acknowledgments and Attributions, What Should Be Acknowledged, Acknowledgments in, Books Dissertations, Dedication or Acknowledgments.

Text book 1: Chapter-3

Module-3	8 Hours
Introduction To Intellectual Property: Role of IP in the Economic and Cultural Development of the Society, IP Governance, IP as a Global Indicator of Innovation, Origin of IP History of IP in India. Major Amendments in IP Laws and Acts in India. Patents: Conditions for Obtaining a Patent Protection, To Patent or Not to Patent an Invention. Rights Associated with Patents. Enforcement of Patent Rights. Inventions Eligible for Patenting. Non-Patentable Matters. Patent Infringements. Avoid Public Disclosure of an Invention before Patenting. Process of Patenting. Process of Patenting. Prior Art Search. Choice of Application to be Filed. Patent Application Forms. Jurisdiction of Filing Patent Application. Publication. Pre-grant Opposition. Examination. Grant of a Patent. Validity of Patent Protection. Post-grant Opposition. Commercialization of a Patent. Need for a Patent Attorney/Agent. Can a Worldwide Patent be Obtained? Do I Need First to File a Patent in India? Patent Related Forms. Fee Structure. Types of Patent Applications. Commonly Used Terms in Patenting. National Bodies Dealing with Patent Affairs. Utility Models**.** **Text book 1: Chapter-4,5,6**	
Module-4	**8 Hours**
Copyrights and Related Rights: Classes of Copyrights. Criteria for Copyright. Ownership of Copyright. Copyrights of the Author. Copyright Infringements. Copyright Infringement is a Criminal Offence. Copyright Infringement is a Cognizable Offence. Fair Use Doctrine. Copyrights and Internet. Non-Copyright Work. Copyright Registration. Judicial Powers of the Registrar of Copyrights. Fee Structure. Copyright Symbol.Validity of Copyright. Copyright Profile of India. Copyright and the word 'Publish'. Transfer of Copyrights to a Publisher. Copyrights and the Word 'Adaptation'. Copyrights and the Word 'Indian Work'. Joint Authorship. Copyright Society. Copyright Board. Copyright Enforcement Advisory Council (CEAC). International Copyright Agreements, Conventions and Treaties. Interesting Copyrights Cases. Trademarks: Eligibility Criteria. Who Can Apply for a Trademark. Acts and Laws. Designation of Trademark Symbols. Classification of Trademarks. Registration of a Trademark is Not Compulsory. Validity of Trademark. Types of Trademark Registered in India. Trademark Registry. Process for Trademarks Registration. Prior Art Search. Famous Case Law: Coca-Cola Company vs. Bisleri International Pvt. Ltd **Text book 1: Chapter-7,8**	
Module-5	**8 Hours**
Industrial Designs: Eligibility Criteria. Acts and Laws to Govern Industrial Designs. Design Rights. Enforcement of Design Rights. Non-Protectable Industrial Designs India. Protection Term. Procedure for Registration of Industrial Designs. Prior Art Search. Application for Registration. Duration of the Registration of a Design. Importance of Design Registration. Cancellation of the Registered Design. Application Forms. Classification of Industrial Designs. Designs Registration Trend in India. International Treaties. Famous Case Law: Apple Inc. vs. Samsung Electronics Co. Geographical Indications: Acts, Laws and Rules Pertaining to GI. Ownership of GI. Rights Granted to the Holders. Registered GI in India. Identification of Registered GI. Classes of GI. Non-Registerable GI. Protection of GI. Collective or Certification Marks. Enforcement of GI Rights. Procedure for GI Registration	

Documents Required for GI Registration. GI Ecosystem in India. Case Studies on Patents. Case study of Curcuma (Turmeric) Patent, Case study of Neem Patent, Case study of Basmati patent. IP Organizations In India. Schemes and Programmes.

Text book 1: Chapter-9,10,11

Course Outcomes(Course Skill Set):

At the end of the course, the student will be able to:

CO1. To know the meaning of engineering research. .(PO – 1,2,3,6.10,11 PSO –1,2)

CO2. To know the procedure of the literature Review and Technical Reading (PO–1,10.11,12 PSO –1)

CO3. To understand the fundamentals of the patent laws and drafting procedure (PO–1,10.11,12 PSO – 1)

CO4. Understanding the copyright laws and subject matters of copyrights and designs **:**(PO– 1,10,11,12 PSO –1)

CO5. Understanding the basic principles of design rights (PO– 1,10,11,12 PSO – 1)

Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.

- Each test shall be conducted for 25 marks

The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks

- Any two assignment methods, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)

- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks. The Internal Assessment Test question paper is designed to attain the different levels of Bloom’s taxonomy as per the outcome defined for the course. Semester-End Examination: Theory SEE will be conducted by University as per the scheduled timetable, with common question

papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.

2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.

3. The students have to answer 5 full questions, selecting one full question from each module. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Textbook:

1. Dr. Santosh M Nejakar, Dr. Harish Bendigeri "Research Methodology and Intellectual Property Rights", ISBN 978-93-5987-928-4, Edition: 2023-24.

Reference Book:

1. David V. Thiel "Research Methods for Engineers" Cambridge University Press, 978-1-107-03488-4
2. Intellectual Property Rights by N.K.Acharya Asia Law House 6th Edition. ISBN: 978-93-81849-30-9

Web links and Video Lectures(e-Resources):

- https://onlinecourses.nptel.ac.in/noc23_ge36
- https://onlinecourses.nptel.ac.in/noc22_ge08
- https://onlinecourses.nptel.ac.in/noc23_ge36
- https://onlinecourses.nptel.ac.in/noc22_ge08
- https://onlinecourses.nptel.ac.in/noc23_ge36

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning(But are not limited to)

- Flipped classroom
- Case Study

Basic VLSI Design			
Course Code	24EC66A	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	3:0:0	**SEE Marks**	50
Credits	03	**Total Marks**	100
Contact Hours	40	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Fundamentals of **Digital Electronics and Logic Design**
- Knowledge of **HDL concepts (Verilog/VHDL basics)**
- Basic understanding of **VLSI Design flow**
- Familiarity with **CMOS digital circuits**
- Basic programming concepts (C/C++ or similar procedural language)
- Understanding of simulation concepts and digital system modelling.

Course objectives:

1. Impart knowledge of MOS transistor theory and CMOS technologies
2. Impart knowledge on architectural choices and performance trade offs involved in designing and realizing the circuits in CMOS technology
3. Cultivate the concepts of subsystem design processes
4. Demonstrate the concepts of CMOS testing

Teaching-Learning Process (General Instructions) The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method(L)does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative(Group) Learning in the class
4. Ask at least three HOTS(Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate ,generalize ,andanalyze information rather than simply recall it.
6. Show the different way to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world and when that's possible,It helps improve the students 'understanding.
8. Incorporate programming examples give number Activity based learning.

Module-1 **8 Hours**

Introduction: ABrief History ,MOS Transistors, MOS Transistor Theory ,Ideal I-V Characteristics, Non ideal I-V Effects,DCTransferCharacteristics

Text 2:1.1,1.3,2.1,2.2, 2.4,2.5

Fabrication: nMOS Fabrication, CMOS Fabrication [P-well process,N well process, Twin tub process], BiCMOS Technology

Text 1: 1.7,1.8,1.10.

Module-2	**8 Hours**

MOS and BiCMOS Circuit Design Processes: MOS Layers, Stick Diagrams, Design Rules and Layout. Basic Circuit Concepts: Sheet Resistance ,Area Capacitances of Layers,Standard Unit of Capacitance, Some Area Capacitance Calculations, Delay Unit ,Inverter Delays, Driving Large Capacitive Loads

Text 3:3.1to3. 3,4.1,4.3-4.8.

Module-3	**8 Hours**

Scaling of MOS Circuits: Scaling Models & Scaling Factors for device Parameters Subsystem Design Processes: Some General considerations, An illustration of Design Processes, Illustration of the Design Processes: Regularity, Design of an ALU Subsystem, The Manchester Carry-chain and Adder Enhancement Techniques

Text 1:5.1,5.2, 7.1,7.2,8.2,8.3, 8.4.1,8.4.2

Module-4	**8 Hours**

Sub system Design: Some Architectural Issues, Switch Logic, Gate(restoring) Logic, Parity Generators, Multiplexers, The Programmable Logic Array (PLA)
Text 1: 6.1to6.3,6.4.1,6.4.3,6.4.6
FPGA Based Systems:Introduction,Basic concepts, Digital design and FPGAs, FPGA based System design, FPGA architecture, Physical design for FPGAs
Text 3:1.1to1.4,3.2,4.8

Module-5	**8 Hours**

Memory, Registers and Aspects of System Timing: SystemTiming Considerations, Some commonly used Storage /Memory elements

Text 1: 9.1,9.2

Testing and Verification: Introduction, Logic Verification, Logic Verification Principles, Manufacturing Test Principles, Design for testability Methodology (UVM), overview of UVM components and phases.

Text 3: 12.1,12.1.1, 12.3, 12.5,12.6

Course outcome (CourseSkillSet)
At the end of the course the student will be able to:
CO1: Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
CO2: Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
CO3: Interpret Memory elements along with timing considerations
CO4: Demonstrate knowledge of FPGA based system design
CO5: Interpret testing and testability issues in VLSI Design
CO6: Analyze CMOS subsystems and architectural issues with the design constraints.

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the regulations; if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

The Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

TextBooks:

1. "Basic VLSI Design"- Douglas A Pucknell & Kamran Eshraghian, PHI, 3rd Edition.

2. "CMOS VLSI Design A Circuits and Systems Perspective ",Neil H E Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.

3. “FPGA Based System Design ”Wayne Wolf, Pearson Education, 2004,Technology and Engineering.

WeblinksandVideoLectures(e-Resources)

- https://nptel.ac.in/courses/117101058
- https://nptel.ac.in/courses/117106093
- https://youtu.be/9SnR3M3CIm4
- https://nptel.ac.in/courses/108/107/108107129/

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning(But are not limited to)

Wherever necessary Cadence/Synopsis/MentaGraphics tools must be used.

1. Write Verilog Code for the following circuits and their TestBench for verification, observe the waveform and synthesize the code with technological library with given Constraints*. Do the initial timing verification with gate level simulation.

i. An inverter

ii. A Buffer

iii. Transmission Gate

iv. Basic/universal gates

v. Flipflop -RS,D, JK,MS, T

vi. Serial & Parallel adder

vii. 4-bitcounter[Synchronous and Asynchronous counter]

2.Design an op amp with given specification *using given differential amplifier Common source and Common Drain amplifier in library**and completing the design flow mentioned below:

a. Draw the schematic and verify the following

i) DC Analysis

ii) AC Analysis

iii) Transient Analysis

b. Draw the Layout and verify the DRC, ERC

c. Check for LVS

d. Extract RC and back annotate the same and verify the Design.

Electronics Communication System			
Course Code	**24EC66B**	**CIE Marks**	**50**
Teaching Hours/Week (L: T:P)	**3:0:0**	**SEE Marks**	**50**
Contact Hours	**40**	**Total Marks**	**100**
Credits	**03**	**Exam Hours**	**3Hrs**
Examination type (SEE)	**Theory**		

Prerequisites: Students should have strong knowledge in the following areas.

- Foundation in differential equations, complex numbers, probability, and Fourier transforms for signal analysis.
- Understanding of electromagnetism, Maxwell's equations, and semiconductor physics.
- Knowledge of passive components (resistors, capacitors, inductors), network theorems, and AC/DC circuit analysis.
- Basics of diodes, transistors (BJTs, MOSFETs), and linear integrated circuits (Op-Amps).
- Understanding time-domain and frequency-domain representations, sampling, and system impulse responses.

Course objectives:

- Describe essential elements of an electronic communication system.
- Understand Amplitude, Frequency & Phase modulations, and Amplitude demodulation.
- Define the sampling theorem and methods to generate pulse modulations.
- Learn the various methods of digital modulation techniques and compare the different schemes.
- Introduce the basic concepts of information theory and coding.

Teaching-Learning Process (General Instructions):

These are sample Strategies, which teachers can use to accelerate the attainment of the various course

outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.

2. Show Video/animation films to explain the evolution of communication technologies.

3. Encourage collaborative (Group) Learning in the class

4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking

5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking

skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.

6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.

7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1	8 Hours

Introduction to Electronic Communications: Historical perspective, Electromagnetic frequency spectrum, Signal and its representation, Elements of electronic communications system, primary communication resources, signal transmission concepts, Analog and digital transmission, Modulation, Concept of frequency translation, Signal radiation and propagation (Text 1: 1.1 to 1.10)

Module-2	8 Hours

Amplitude Modulation Techniques: Types of analog modulation, Principle of amplitude modulation, AM power distribution, Limitations of AM, (TEXT 1: 4.1, 4.2, 4.4, 4.6)

Angle Modulation Techniques: Principles of Angle modulation, Theory of FM-basic Concepts, Theory of phase modulation (TEXT1: 5.1, 5.2, 5.5)

Module-3	8 Hours

Sampling Theorem and Pulse Modulation Techniques: Digital Versus Analog Transmissions, Sampling Theorem, Classification of pulse modulation techniques, PAM, PWM, PPM, PCM, Quantization of signals (TEXT 1: 7.2 to 7.8)

Module-4	8 Hours

Digital Modulation Techniques: Types of digital Modulation, ASK, FSK, PSK, QPSK. (TEXT 1: 9.1 to 9.5)

Information Theory, Source and Channel Coding: Information, Entropy and its properties, Shannon,- Hartley Theorem, Objectives of source coding, Source coding technique, Shannon source coding theorem, Channel coding theorem, Error Control and Coding. [Text1: 10.1,10.2, 10.11.2, 11.1 to 11.3, 11.8, 11.9, 11.12]

Module-5	8 Hours

Evolution of wireless communication systems: Brief History of wireless communications, Advantages of wireless communication, disadvantages of wireless communications, wireless network generations, Comparison of wireless systems, Evolution of next generation networks, Applications of wireless communication (TEXT 2: 1.1 to 1.7)

Principles of Cellular Communications: Cellular terminology, Cell structure and Cluster, Frequency reuse concept, Cluster size and system capacity, Method of locating cochannel cells, Frequency reuse distance (TEXT 2: 4.1 to 4.7)

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Describe the scheme and concepts of radiation and propagation of communication signals through air**.(PO-1,2,,3,PSO-1,2)**
2. Understand the AM and FM modulation techniques and represent the signal in time and frequency domain relations. **(PO-1,2,5,PSO-1,2)**
3. Understand the process of sampling and quantization of signals and describe different methods to generate digital signals. **(PO-1,2,3,5 PSO-1,2)**
4. Describe the basic digital modulation techniques, channel capacity, source coding technique and the channel coding. **(PO-1,2,3,PSO-1,2)**
5. Compare the different wireless communication systems and describe the structure of cellular communication. **(PO-1,2,3,PSO-1,2)**

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Book:

1. T L Singal, Analog and Digital Communications, McGraw Hill Education (India) Private Limited,
   2012, 0-07-107269-1.
2. T L Singal, Wireless Communications, McGraw Hill Education (India) Private Limited, 2016,

Reference Books :

1. Simon Haykin & Michael Moher, Communication Systems, 5th Edition, John Wiley, India Pvt. Ltd, 2010,
   ISBN: 978-81-265-2151-7.
2. Herbert Taub, Donald L Schilling, Goutam Saha, "Principles of Communication systems", 4th Edition, Mc
   Graw Hill Education (India) Private Limited, 2016. ISBN: 978-1-25-902985-1
3. Simon Haykin, "Digital Communication Systems", John Wiley & sons, 2014, ISBN 978-81-265-4231-4

Web links and Video Lectures (e-Resources):

- Communication Engineering **https://nptel.ac.in/courses/117102059**

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning (But are not limited to):

- Seminar
- Flipped classroom
- Assessment Methods Marks (opt two Learning Activities)
- Quiz
- Assignment

Digital System Design using Verilog			
Course Code	24EC66C	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	3:0:0	**SEE Marks**	50
Credits	03	**Total Marks**	100
Contact Hours	40	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on:

- Basic knowledge of Digital Electronics (combinational and sequential circuits)
- Understanding of Boolean algebra and logic gates
- Fundamentals of Verilog HDL concepts

Course Objectives:

This course will enable students to:

- Learn different Verilog HDL constructs.
- Familiarize the different levels of abstraction in Verilog.
- Understand Verilog Tasks and Functions.
- Understand Timing and Delay Simulation.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of combinational and sequential circuits
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.
- Give Programming Assignments.

Module-1	8 Hours
Overview of Digital Design with Verilog HDL: Evolution of Computer-Aided Digital Design (CAD), Emergence of HDLs, Typical Design flow, Importance of HDLs, Popularity of Verilog HDL, Trends in HDLs. Introduction to ASIC Vs FPGA Design flow, Overview of FPGA Architecture (Text 1: 1.1 to 1.6) **Hierarchical Modeling Concepts:** Design Methodologies, Top-down and Bottom-up design methodology, Modules, Instances, Components of a Simulation, Design Block, Stimulus Block (Test Bench) with example. (Text 1:2.1 to 2.6)	
Module-2	**8 Hours**
Basic Concepts: Lexical Conventions, Data Types, System Tasks, Compiler Directives. (Text 1: 3.1 to 3.3) **Modules and Ports:** Modules, Ports, Connecting Ports, Hierarchical Names. (Text 1: 4.1 to 4.3)	
Module-3	**8 Hours**
Gate-Level Modeling: Gate Types-Modeling using basic Verilog gate primitives, Description of AND/OR and BUF/NOT type gates. Gate Delays-Rise, Fall and Turn-Off Delays, Min, Max and Typical Delays. (Text1: 5.1, 5.2) **Dataflow Modeling:** Continuous assignments, Delay Specification, Expressions, Operators, Operands, Operator Types, Examples (Text 1: 6.1 to 6.5)	
Module-4	**8 Hours**
Behavioral Description: Structured Procedures, Initial and Always statements, Procedural Assignments Blocking and Non-Blocking statements, Conditional statements, Multiway Branching, Loops, Sequential and Parallel blocks, Examples-4-to-1 Multiplexer, 4-bit Counter. (Text 1: 7.1, 7.2, 7.4, 7.5, 7.6, 7.7, 7.9.1, 7.9.2)	
Module-5	**8 Hours**
Structural Description: Highlights of Structural Descriptions, Organization of Structural Description, Binding (Text 2: 4.1, 4.2, 4.3, Listings 4.1 to 4.13 only Verilog) **Tasks and Functions:** Differences between Tasks and Functions, Declaration and Invocation, Examples (Text 1: 8.1, 8.2, 8.2.1, 8.2.2, 8.3, 8.3.1, 8.3.2)	

Course Outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Understand the Verilog HDL design flow.(PO – 1,2 ; PSO – 1)

CO2: Apply the basic concepts of Verilog HDL programming.(PO – 1, 2 ; PSO – 1)

CO3: Write Verilog programs in Gate, Dataflow, Behavioral and Structural modeling levels of abstraction.(PO – 1, 2, 3 ; PSO – 1, 2)

CO4: Write programs effectively using Verilog Tasks and Functions.(PO – 2, 3 ; PSO – 1, 2)

CO5: Perform Timing and Delay Simulation.(PO – 1, 2, 5 ; PSO – 2)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks).
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

The Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with 3. a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books

1. “Verilog HDL: A Guide to Digital Design and Synthesis”, Samir Palnitkar, Pearson education, Second edition. 1.
2. “HDL programming (VHDL and Verilog)”, Nazeih M Botros, John Wiley India Pvt. Ltd., 2. 2008.

Reference Books:

1. Donald E. Thomas, Philip R. Moorby, “The Verilog Hardware Description Language”, Springer Science+Business Media, LLC, Fifth edition.
2. Michael D. Ciletti, “Advanced Digital Design with the Verilog HDL” Pearson (Prentice Hall), Second edition.

3. Padmanabhan, Tripura Sundari, “Design through Verilog HDL”, Wiley, 2016 or earlier

Web links and Video Lectures(e-Resources):

- **https://www.youtube.com/watch?v=Xx4RgERSiqk**
- **https://www.youtube.com/watch?v=vTeFdcG5zog**
- **https://www.youtube.com/watch?v=-Cax0OvDr04**

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning(But are not limited to)

- Flipped classroom
- Programming Assignment
- Group Discussion/Quiz.
- Demonstration of Verilog and FPGA concepts.
- Case Study on small design and implementation on FPGA's.

Sensors and Instrumentation			
Course Code	24EC66D	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	3:0:0	**SEE Marks**	50
Credits	03	**Total Marks**	100
Contact Hours	40	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Basic Electrical
- Basic Electronics

Course Objectives:

- Understand various technologies associated in manufacturing of sensors
- Acquire knowledge about types of sensors used in modern digital systems
- Get acquainted about material properties required to make sensors
- Understand types of instrument errors and circuits for multirange Ammeters and Voltmeters.
- Describe principle of operation of digital measuring instruments and Bridges.
- Understand the operations of transducers and instrumentation amplifiers.

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Project based Teaching

Module-1 **8 Hours**

Principles of Measurement: Static Characteristics, Error in Measurement, Types of Static Error. Multirange Ammeters, Multirange voltmeter.

Text Book 1.2-1.6, 2:3.2,4.4

Digital Voltmeter: Ramp Technique, Dual slope integrating Type DVM, Direct Compensation type and Successive Approximations type DVM

Text Book 2: 5.1-5.3, 5.5,5.6)

Module-2 **8 Hours**

Digital Multimeter: Digital Frequency Meter and Digital Measurement of Time, Function Generator, Digital storage Oscilloscope.

Bridges: Measurement of resistance: Wheatstone's Bridge, AC Bridges – Anderson Bridge, Capacitance and Inductance Comparison bridge, Wien's bridge.

Text Book 2: refer 6.2,6.3 up to 6.3.2, 6.4 up to 6.4.2, 8.8,8.32, 11.2, 11.8 -11.10, 11.14.

Module-3 **8 Hours**

Transducers: Introduction, Electrical Transducer, Resistive Transducer, Resistive position Transducer, Resistance Wire Strain Gauges, Resistance Thermometer, Thermistor, LVDT.

Text Book 2:13.1-13.3,13.5, 13.6 up to 13.6.1,13.7,13.8,13.11.
Instrumentation Amplifier using Transducer Bridge: Temperature indicators using Thermometer, Light Intensity meter Analog Weight Scale

Text Book 2:14.3.3, 14.4.1,14.4.2, 14.4.3.

Module-4 **8 Hours**

Introduction to sensor-based measurement systems:
General concepts and terminology, sensor classification, Primary Sensors- Temperature Sensors-Bimetal, Pressure sensors, Flow velocity and Flowrate sensors, Level sensors, acceleration and Inclination sensors, velocity sensors, material for sensors.

Text Book 1-1.1, 1.7-1.8

Module-5 **8 Hours**

Self-generating Sensors: Thermoelectric sensors -Thermocouples, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, Electrochemical sensors.

Text Book 1 :6.1.1, 6.1.3, 6.2.1, 6.2.2, 6.2.3, 6.3.1, 6.3.2, 6.3.3, 6.4.1,6.4.2,6.5

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:
CO1: Apply Principles of Measurement and Error Analysis in Sensor Systems. (PO – 1,2,3, PSO – 1,3)
CO2: Gain Proficiency in the Use of Bridges and Digital Measurement Instruments. (PO – 1,2,3, PSO – 1,3)

CO3: Analyze Sensor-Based Transducer Systems for Measurement Applications. (PO – 1,2,3, PSO – 1,3)
CO4: Understand the Fundamental Concepts of Sensors and Measurement Systems. (PO –1,2,3, PSO – 1,3)
CO5: Demonstrate Knowledge of Self-Generating Sensors and Their Applications.(PO – 1,2,3, PSO – 1,3)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Textbook:

1. "Sensors and Signal Conditioning", Ramon Pallas Areny, John G. Webster,2nd edition, John Wiley
   and Sons,2000
2. H.S.Kalsi, "Electronic Instrumentation", Mc Graw Hill,3rd Edition and 4th Edition,2012, ISBN:9780070702066.

Reference Books:

1. DavidA. Bell, "Electronic Instrumentation & Measurements", Oxford University Press PHI 2ndEdition, 2006, ISBN 81-203-2360-2.
2. D. Helfrick and W.D. Cooper, "Modern Electronic Instrumentation and Measuring Techniques", Pearson, 1stEdition, 2015, ISBN: 9789332556065.

Web links and Video Lectures(e-Resources):

- https://www.youtube.com/watch?v=9EsOFiP1J2E
- https://www.youtube.com/watch?v=hdaVgptDQAc
- https://www.youtube.com/watch?v=HY39LA6H-Lo
- https://www.youtube.com/watch?v=c-Ioo_Q9__Q
- https://www.youtube.com/watch?v=GR8WywKMiiQ
- https://www.youtube.com/watch?v=zkixSsT2p7w
- https://www.youtube.com/watch?v=nar2I82bJvU

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning not limited to the following

- Flipped classroom
- Assessment Methods for 25 Marks (opt two Learning Activities)
  - Quiz
  - Assignment
  - MOOC Assignment for selected Module

Indian Knowledge System			
Course Code	24IKS69	**CIE Marks**	100
Teaching Hours/Week (L: T: P)	1:0:0	**SEE Marks**	-
Credits	NCMC – Non Credit Mandatory Course (Completion of the course shall be mandatory for the award of degree)	**Total Marks**	100
Contact Hours	28	**Exam Hours**	-
Examination type (SEE)	NA		

Course objectives:

- To facilitate the students with the concepts of Indian traditional knowledge and to make them understand the Importance of roots of knowledge system.
- To make the students understand the traditional knowledge and analyse it and apply it to their day-to-day life.

Module-1	**5 Hours**
Introduction to Indian Knowledge Systems (IKS): Overview, Vedic Corpus, Philosophy, Character scope and importance, traditional knowledge vis-a-vis indigenous knowledge, traditional knowledge vs. western knowledge.	
Module-2	**5 Hours**
Traditional Knowledge in Humanities and Sciences: Lingistics, Number and measurements-Mathematics, Chemistry, Physics, Art, Astronomy, Astrology, Crafts and Trade in India and Engineering and Technology.	
Module-3	**5 Hours**
Traditional Knowledge in Professional domain: Town planning and architecture-Construction, Health, wellness and Psychology-Medicine, Agriculture, Governance and public administration, United Nations Sustainable development goals.	

Course outcomes (Course Skill Set)

At the end of the course, the student will be able to:

CO1. Provide an overview of the concept of the Indian Knowledge System and its importance.PO-1,7,11

CO2. Appreciate the need and importance of protecting traditional knowledge. PO6

CO3. Recognize the relevance of Traditional knowledge in different domains.PO-3,4

CO4. Establish the significance of Indian Knowledge systems in the contemporary world.PO6

Reference Books

1	**Introduction to Indian Knowledge System- concepts and applications**, B Mahadevan, Vinayak Rajat Bhat, Nagendra Pavana R N, 2022, PHI Learning Private Ltd, ISBN-978-93-91818-21-0
2	**Traditional Knowledge System in India**, Amit Jha, 2009, Atlantic Publishers and Distributors (P) Ltd., ISBN-13: 978-8126912230,
3	**Knowledge Traditions and Practices of India**, Kapil Kapoor, Avadesh Kumar Singh, Vol. 1, 2005, DK Print World (P) Ltd., ISBN 81-246-0334,

Suggested Web Links:

1.	https://www.youtube.com/watch?v=LZP1StpYEPM
2.	http://nptel.ac.in/courses/121106003/

3.	http://www.iitkgp.ac.in/department/KS;jsessionid=C5042785F727F6EB46CBF432D7683B63 (Centre of Excellence for Indian Knowledge System, IIT Kharagpur)
4.	https://www.wipo.int/pressroom/en/briefs/tk_ip.html
5.	https://unctad.org/system/files/official-document/ditcted10_en.pdf
6.	http://nbaindia.org/uploaded/docs/traditionalknowledge_190707.pdf
7.	https://unfoundation.org/what-we-do/issues/sustainable-development goals/?gclid=EAIaIQobChMInp-Jtb_p8gIVTeN3Ch27LAmPEAAYASAAEgIm1vD_BwE

ASSESSMENT AND EVALUATION PATTERN	
WEIGHTAGE	**100% (CIE)**
QUIZZES	
Quiz-I	Each quiz is evaluated for 10 marks adding up to **20 Marks**
Quiz-II	
THEORY COURSE - (Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating)	
Test – I	Each test will be conducted for 25 Marks adding upto 50 marks. Final test marks will be reduced to **40 Marks**
Test – II	
EXPERIENTIAL LEARNING	**40**
Case Study-based Teaching-Learning	**--**
Sector wise study & consolidation (viz., Engg. Semiconductor Design, Healthcare & Pharmaceutical, FMCG, Automobile, Aerospace and IT/ ITeS)	**--**
Video based seminar (4-5 minutes per student)	**--**
Maximum Marks for the Theory	**--**
Practical	**--**
Total Marks for the Course	**100**