Analog and Digital Electronics laboratory			
Course Code	24ECL35	**CIE Marks**	50
Teaching Hours/Week (L: T:P)	0:0:2	**SEE Marks**	50
Credits	01	**Total Marks**	100
Contact Hours	12	**Exam Hours**	3
Examination type (SEE)	Practical		

Prerequisites:

The students should have knowledge on

- BJTs, FETs, and Frequency response and their biasing.
- Basics of Operational amplifiers (op-amp applications)
- Logic gates and Boolean algebra
- Combinational and Sequential circuits: Adders, multiplexers, encoders, Flip-flops, counters, shift registers

Course Objectives:

Understand the electronic circuit schematic and its working

- Realize and test amplifier and oscillator circuits for the given specifications
- Realize the op-amp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers.
- Design and test the combinational and sequential logic circuits for their functionalities.
- Use the suitable ICs based on the specifications and functions.

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Demonstration based

LIST OF EXPERIMENTS

1	Design and the BJT common emitter voltage amplifier with feedback and determine the gain- bandwidth product, input and output impedances.
2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator
3	Design and set up the circuits using opamp: i) Adder, ii) Integrator, iii) Differentiator
4	Design and test Monostable and Astable Multivibrator using 555 Timer

5	Design and implement (a) Half Adder & Full Adder using basic gates and NAND gates, (b) Half subtractor & Full subtractor using NAND gates,
7	Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii)T Flip-Flop
8	Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter
9	Realize a) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop b) Mod-N Counter using IC7490 / 7476 c) Synchronous counter using IC74192
10	Design and Simulate inverting and non-inverting amplifier with op-amp using Suitable simulation software (Matlab Simulink/Pspice/Matlab)
11	Design and simulate RC Phae shift Oscillator using suitable simulation software (Matlab Simulink/Pspice/Matlab)
12	Design of simulate Comparator using suitable simulation software (Matlab Simulink/Pspice/Matlab)
	Course outcomes (Course Skill Set): At the end of the course the student will be able to: **CO1**. Design and analyze the BJT/FET amplifier and oscillator circuits.(PO-1,2,3,PSO-1,2) **CO2.** Design and test Op-amp circuits to realize the mathematical computations, DAC and precision rectifiers. .(PO-1,2,3,PSO-1,2) **CO3**.Demonstrate the basic circuit experiments using 555 timer.(PO-1,2,3,PSO-1,2) **CO4.** Design and test the sequential and combinational logic circuits for the given specifications. .(PO-1,2,3,PSO-1,2,3) **CO5**. Design and Simulate the experiments using Op-amp with simulation tool(Matlab simulink/Pspice/LTspice.) .(PO-1,2,3,PSO-1,2,3) **Assessment Details (both CIE and SEE):** The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. **Continuous Internal Evaluation (CIE):** CIE marks for the practical course are 50 Marks. The split-up of CIE marks for record/ journal and test are in the ratio 60:40. • Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session. • Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks. • Total marks scored by the students are scaled down to 30 marks (60% of maximum marks). • Weightage to be given for neatness and submission of record/write-up on time. • Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.

- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to 20 marks (40% of the maximum marks).
- The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- SEE shall be conducted jointly by the two examiners one from other institute and one from the same institute, examiners are appointed by the Board of Examiner.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination.
- These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University. All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners) Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual", 5th Edition, 2009, Oxford University Press.
2. Albert Malvino, David J Bates, Electronic Principles, 7th Edition, Mc Graw Hill Education, 2017.
3. Fundamentals of Logic Design, Charles H Roth Jr., Larry L Kinney, Cengage Learning, 7th Edition

Web links and Video Lectures(e-Resources):

- **https://www.youtube.com/watch?v=ES-kcNR4Ln0&list=PLXb3r5nv8_1W6sIWl6CWFOv-F31sAt9j_&index=7**
- **https://www.youtube.com/watch?v=idJEMYhrIfs**

- https://www.youtube.com/watch?v=DBTna2ydmC0
- https://www.youtube.com/watch?v=JQBRzsPhw2w

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning:

- Mini Projects
- Hands-on

Virtual Lab Link:

- https://aec-iitkgp.vlabs.ac.in/List%20of%20experiments.html

Mathematics-III for EEE Stream			
Course Code	24EC31	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	3:2:0	**SEE Marks**	50
Credits	04	**Total Marks**	100
Contact Hours	55	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Basics of differentiation and Integration
- Basic Statistics
- Problem-Solving Skills

Course Objectives:

- Learn to use the Fourier series to represent periodical physical phenomena in engineering analysis and to enable the student to express non-periodic functions to periodic functions using the Fourier series and Fourier transforms.
- Analyze signals in terms of Fourier transforms on some commonly encountered hypotheses.
- Develop the knowledge of solving differential equations and their applications in Electronics & Communication engineering.
- To find the association between attributes and the correlation between two variables.

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Demonstration based Teaching

Module-1 **11 Hours**

Fourier series and practical harmonic analysis: Periodic functions, Dirichlet's condition. Fourier series expansion of functions with period 2π and with arbitrary period: periodic rectangular wave, Half-wave rectifier, rectangular pulse, Saw tooth wave. Half-range Fourier series. Triangle and half range expansions, Practical harmonic analysis, variation of periodic current.

Text Book:1;10.1-10.8. Text Book 2:11.3

Module-2 **11 Hours**

Infinite Fourier Transforms: Infinite Fourier transforms, Fourier cosine and sine transforms, Inverse Fourier transforms, Inverse Fourier cosine and sine transforms, discrete Fourier transform (DFT).

Text Book 1, 22.1-22.5. Text Book 2:11.9

Module-3 **11 Hours**

Z Transforms:1 Definition, Z-transforms of basic sequences and standard functions. Properties: Linearity,
scaling, first and second shifting, multiplication by n. Initial and final value theorem. Inverse Z- transforms. Application to difference equations.

Text Book 1:23.1--23.8, 23.11, 23.15, 23.16

Module-4	11 Hours
Ordinary Differential Equations of Higher Order: Higher-order linear ODEs with constant coefficients - Inverse differential operator, problems. Linear differential equations with variable Coefficients-Cauchy's and Legendre's differential equations–Problems. Application of linear differential equations to L-C circuit and L-C-R circuit. **Text Book 1,13.1-13.4 and 13.6, 13.9, 14.5**	
Module-5	**11 Hours**
Curve fitting, Correlation, and Regressions: Principles of least squares, Curve fitting by the method of least squares in the form $y = a + bx$, $y = a + bx + cx^2$, and $y = ax^b$. Correlation, Coefficient of correlation, Lines of regression, Angle between regression lines, standard error of estimate, rank correlation. **Text Book 1:24.1and 24.4-24.6, 25.12-25.16**	

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Demonstrate the Fourier series to study the behavior of periodic functions and their applications in system communications, digital signal processing, and field theory. (PO – 1,2,3)

CO2: To use Fourier transforms to analyze problems involving continuous-time signals (PO – 1,2,3)

CO3: To apply Z-Transform techniques to solve difference equations. (PO – 1,2,3)

CO4: Understand that physical systems can be described by differential equations and solve such equations. (PO – 1,2,3)

CO5: Make use of correlation and regression analysis to fit a suitable mathematical model for statistical data. (PO – 1,2,3)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the regulations; if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two

assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)

- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Textbook:

1. **B. S. Grewal**: "Higher Engineering Mathematics", Khanna Publishers, 44thEd., 2021.
2. **E. Kreyszig**: "Advanced Engineering Mathematics", John Wiley & Sons, 10thEd., 2018.

Reference Books:

1. **V. Ramana:** "Higher Engineering Mathematics" McGraw-Hill Education, 11th Ed., 2017
2. **Srimanta Pal & Subodh C.Bhunia**: "Engineering Mathematics" Oxford University Press,3rd Ed., 2016.
3. **H. K. Dass and Er. Rajnish Verma:** "Higher Engineering Mathematics" S. Chand Publication, 3rd Ed., 2014.
4. **N.P Bali and Manish Goyal**: "A Textbook of Engineering Mathematics" Laxmi Publications, 10thEd., 2022.
5. **C. Ray Wylie, Louis C. Barrett:** "Advanced Engineering Mathematics" McGraw–Hill Book Co., New York, 6thEd., 2017.
6. **Gupta C.B, Sing S.R and Mukesh Kumar:** "Engineering Mathematic for Semester I and II", McGraw Hill Education(India) Pvt. Ltd 2015.
7. **James Stewart: "**Calculus" Cengage Publications, 7thEd., 2019.

Web links and Video Lectures(e-Resources):

- http://nptel.ac.in/courses.php?disciplineID=111
- http://www.class-central.com/subject/math(MOOCs)
- http://academicearth.org/
- http://www.bookstreet.in.

• VTU EDUSAT PROGRAMME – 20
Activity Based Learning (Suggested Activities in Class)/Practical Based Learning • Programming Assignment • Seminars

Network Analysis			
Course Code	**24EC32**	CIE Marks	50
Teaching Hours/Week (L: T: P)	3:2:0	SEE Marks	50
Total Hours of Pedagogy	55	Total Marks	100
Credits	04	Exam Hours	3
Examination type (SEE)	Theory		

Prerequisites:

- The students should have knowledge on
- Basic Electrical Concepts
- Mathematics
- Basic Physics

Course objectives:

- Apply mesh and nodal techniques to solve an electrical network and solve different problems related to Electrical circuits using Network Theorems and Two port network.
- Examine the behavior of RL, RC, and RLC circuits under different excitation conditions.
- To Familiarize with the use of Laplace transforms to solve network problems.
- Study and analyze two port network parameters and gain proficiency in resonance phenomena.
- Utilize graph theory concepts for circuit modeling and optimization.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.

Module – 1 (11 Hours)

Network Theorems: KCL and KVL for electric circuits, Superposition, Millman's theorems, Thevenin's and Norton's theorems, Maximum Power transfer theorem.

Module – 2 (11 Hours)

Transient behavior and initial conditions: Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations.

Module – 3 (11 Hours)

Laplace Transformation & Applications: Solution of networks, step, ramp and impulse responses, waveform Synthesis.

Module – 4 (11 Hours)

Resonance:
Series Resonance: Variation of Current and Voltage with Frequency, Selectivity and Bandwidth, Q-Factor, Circuit Magnification Factor, Selectivity with Variable Capacitance, Selectivity with Variable Inductance.

Parallel Resonance: Selectivity and Bandwidth, Maximum Impedance Conditions with C, L and f Variable, current in Anti-Resonant Circuit.

Module – 5 (11 Hours)

Two port network parameters: Definition of Z, Y, h and Transmission parameters, modelling with these parameters, relationship between parameters sets.

Graph Theory in Network Analysis – Basic graph terminology, Tree and co-tree, Incidence matrix, tie-set & cut-set concepts, Concept of duality.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Evaluate the branch currents and node voltages of any given electrical circuit by the application of various network theorems.
2. Apply initial and final conditions to analyze transient behavior of the network.
3. Apply Laplace transform techniques to solve the given network.
4. Determine the resonant circuits for the given frequency and model the two port network parameters in terms of Z, Y, h and T parameters.
5. Analyze various graph structures for the given electrical networks.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of

40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Books:

1. M. E. Van Valkenburg, "Network Analysis", Prentice Hall of India, 3rd edition, 2019.
2. R R Singh, "Network Analysis and Synthesis", 2nd Edition, TMH Publication, 2019.
3. A Chakrabarti, "Circuit Theory (Analysis and Synthesis)", Dhanpat Rai & Co., 2013.

Reference Books:

4. W H Hayt, J M Kemmerly and S M Durbin – "Engineering Circuit Analysis", TMH Publication, 6th Edition, 2011.
5. Charles K Alexander and Mathew NO Sadiku – "Fundamentals of Electric Circuits", Tata McGraw-Hill, 3rd Edition, 2009.
6. J. David Irwin, R. Mark Nelms – "Basic Engineering Circuit Analysis", 8th Edition, John Wiley, 2006.

YouTube Video Links:

1. https://www.youtube.com/watch?v=ouQoab7GVRQ&list=PLbRMhDVUMngfNnABo5mre45ZbHqJE2sUn&index=51-58
2. https://www.youtube.com/watch?v=YoYBPARDh8k&list=PLbRMhDVUMngfNnABo5mre45ZbHqJE2sUn&index=9-24

3. https://www.youtube.com/watch?v=c0cx6lmA8-0&list=PLbRMhDVUMngfNnABo5mre45ZbHqJE2sUn&index=43-50
4. https://www.youtube.com/watch?v=plv9ovmwHmA&list=PLbRMhDVUMngfNnABo5mre45ZbHqJE2sUn&index=70-77
5. https://www.youtube.com/watch?v=0BQ2yyC6Lc8&list=PLbRMhDVUMngfNnABo5mre45ZbHqJE2sUn&index=58-67

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Circuit Construction with Breadboard
- Mesh and Nodal Analysis Puzzle
- Quiz

Electronic Principles and Circuits			
Course Code	24EC33	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	3:0:0	**SEE Marks**	50
Credits	03	**Total Marks**	100
Contact Hours	40	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Basics of semiconductor physics
- Basic Multivibrators
- MOSFETs

Course Objectives:

- To design and analyse the BJT circuits as an amplifier and voltage regulation.
- To design of MOSFET Amplifiers and analyse the basic amplifier configurations using small signal equivalent circuit models
- To design of operational amplifiers circuits as Comparators, DAC and filters.
- To understand the concept of positive and negative feedback.
- To analyze Power amplifier circuits in different modes of operation.
- To construct Feedback and Oscillator circuits using FET.
- To understand the thyristor operation and the different types of thyristors.

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Demonstration based Teaching

Module-1 **8 Hours**

TRANSISTOR BIASING: Voltage Divider Bias, VDB Analysis, VDB Load line and Q point, Two supply Emitter Bias, Other types of Bias.

BJT AC MODELS: Base Biased Amplifier, Emitter Biased Amplifier, CC Amplifier, Output Impedance ,Small Signal Operation, AC Beta, AC Resistance of the emitter diode, Two transistor models, Analyzing an amplifier.

VOLTAGE AMPLIFIERS: Voltage gain, Loading effect of Input Impedance.

Text Book: Text1: Chapter8: 8-1,8-3,8-4,8-5 Chapter 9: 9-1,9-2,9-3,9-4,9-5,9-6,9-7 Chapter 10: 10-1,10-2 Chapter 11: 11-1,11-2.

Module-2	9 Hours
MOSFET: Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor. Small signal operation and modelling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model. **MOSFET Amplifier configuration:** Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance, The Common Gate Amplifier, Source follower. **Text Book**: Text2: Chapter 5: 5.7.1,5.7.2, 5.7.3, 5.5.1, 5.5.2,5.5.3, 5.5.5, 5.5.6,5.5.7, 5.6.1,5.6.2,5.6.3, 5.6.4, 5.6.5.	
Module-3	**7 Hours**
NEGATIVE FEEDBACK: Four Types of Negative Feedback, VCVS Voltage gain, Other VCVS Equations, ICVS Amplifier, VCIS Amplifier, ICIS Amplifier (No Mathematical Derivation). **ACTIVE FILTERS:** Ideal Responses, First Order Stages, VCVS Unity Gain Second Order Low pass Filters, VCVS Equal Component Low Pass Filters, VCVS High Pass Filters, MFB Bandpass Filters, Bandstop Filters. **Text Book**: Text1: Chapter 19: 19-1 to 19-6, Chapter 21: 21-1,21-4,21-5,21-7,21-8,21-9,21-10.	
Module-4	**8 Hours**
LINEAR OPAMP CIRCUITS: Summing Amplifier, D/A Converter **NONLINEAR OP-AMP CIRCUITS:** Comparator with zero reference, Comparator with non-zero references. Comparator with Hysteresis**,** Integrators, differentiators**.** **OSCILLATOR:** Theory of Sinusoidal Oscillation, The Wien-Bridge Oscillator, RC Phase Shift Oscillator, The Colpitts Oscillator, Hartley Oscillator. **MULTIVIBRATORS:** The 555 timer- Monostable Operation, Astable Operation. **Text Book**: Text1: Chapter 20: 20-6, 20-7 Chapter 22: 22-1,22-2,22-3,22-5,22-10 Chapter 23: 23-1,23-2,23-3,23-4,23-5,23-7.	
Module-5	**8 Hours**
POWER AMPLIFIERS: Amplifier terms, Two load lines, Class A Operation, Class B operation, Class B push pull amplifiers, Class C Operation. **THYRISTORS:** The four layer Diode, SCR, SCR Phase control, Bidirectional Thyristors, IGBTs, Other Thyristors. **Text Book** :Text1: Chapter 12:12-1,12-2,12-3,12-4,12-5,12-8 Chapter 15:15-1,15-2,15-4,15-5,15-6,15-7.	
Course outcomes (Course Skill Set): At the end of the course, the student will be able to: **CO1:** Analyze the characteristics of BJTs and FETs for switching and amplifier circuits. (PO – 1,2,3,PSO – 1,2) **CO2:** Design and analyze amplifiers and oscillators with different circuit configurations and biasing conditions. (PO – 1,2,3, PSO – 1,2) **CO3:** Apply the feedback topologies and approximations in the design of amplifiers and oscillators. (PO – 1,2,3,4 PSO – 1,2) **CO4:** Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers. (PO – 1,2,3, PSO – 1,2) **CO5:** Analyze the power electronic device components and its functions for basic power electronic circuits. (PO – 1,2,3, PSO – 1,2)	

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the regulations; if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Proposed activities to be carried out for 10 marks of CIE:

Using suitable simulation software, perform the operation of the following circuits:

1. Design and test i)Emitter Follower ii)Darlington connection
2. Design and Plot i) The transfer and drain characteristics of a JFET
   ii) The transfer and drain characteristics of n-channel MOSFET
3. Design and test i) Low Pass Filter ii) High Pass Filter iii) Band Pass Filter
4. Design and test i) Precision Half wave and full wave rectifiers using Op-amp
   ii) RC phase shift oscillator
5. Design and test Full wave Controlled rectifier using RC triggering circuit.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.

3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Textbook:

1. Albert Malvino, David J Bates, Electronic Principles, 7th Edition, Mc Graw Hill Education, 2017, ISBN:978-0- 07-063424-4.
2. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6th Edition, Oxford, 2015.ISBN:978-0-19-808913-1

Reference Books:

1. Boylestad and Louis Nashelsky, Electronics devices and Circuit theory, 10/11thEdition, Pearson.
2. D Roy Choudhury and Shail B Jain, Linear Integrated Circuits, 5th Edition, New age International Limited, 2015**.**

Web links and Video Lectures(e-Resources):

- Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015.
- Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.
- https://onlinecourses.nptel.ac.in/noc25_ee103
- https://onlinecourses.nptel.ac.in/noc25_ee157
- https://ocw.mit.edu/courses/6-002-circuits-and-electronics-spring-2007/
- https://www.vlab.co.in/broad-area-electronics-and-communications
- https://semesterlearning.com/product/principles-and-applications-of-electronic-devices-and-circuits/
- https://onlinecourses.nptel.ac.in/noc20_ee32/preview
- https://nit-edu.org/wp-content/uploads/2021/09/Electrical-Electronic-Principles-Technology-John-Bird-2nd-Ed.pdf
- https://www.coursera.org/courses?query=circuits

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Role Play
- Flipped classroom
- Assessment Methods for 25 Marks (opt two Learning Activities)
  - Case Study
  - Assignment & online certifications
  - Simulation of circuits using suitable software

Digital System Design using Verilog			
Course Code	24EC34	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	3:0:2	**SEE Marks**	50
Credits	04	**Total Marks**	100
Contact Hours	40 Hours (Theory) + 10 -12 Lab Slots	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Number systems (Binary, Decimal, Hex, Octal)
- Logic gates (AND, OR, NOT, NAND, NOR, XOR, XNOR) and truth tables
- Boolean algebra
- Basic programming concepts

Course Objectives:

- To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques.
- To impart the concepts of designing and analyzing combinational logic circuits.
- To impart design methods and analysis of sequential logic circuits.
- To impart the concepts of Verilog HDL-data flow, behavioural and structural models for the design of digital systems.

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Demonstration based Teaching

Module-1 **8 Hours**

PRINCIPLES OF COMBINATIONAL LOGIC: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-up to 4 variables, Quine-McCluskey Minimization Technique. Quine - McCluskey using Don't Care Terms.
Text Book: Text 1 – Chapter 3-3.1 to 3.5

Module-2 **8 Hours**

COMBINATIONAL LOGIC CIRCUITS: Binary Adders and Subtractors, Comparators, Decoders, Encoders, Multiplexers, Demultiplexer, Programmable Logic Devices – PLAs, PAL, PROMs
Text Book: Text 2 - Chapter 5: 5.1 to 5.10

Module-3	9 Hours
FLIP-FLOPS AND ITS APPLICATIONS: Basic bi-stable element, Latches- SR Latch using NAND gates, D Latch, Gated D Latch, The Master-Slave Flip-flops (Pulse-Triggered flip-flops):SR flip- flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, J K, D and SR flip-flops. **Text Book**: Text 2 – Chapter 6: 6.1 to 6.4, 6.6 to 6.9	
Module-4	**8 Hours**
INTRODUCTION TO VERILOG: HDL basic Concepts, Structure of Verilog module, Operators, Data Types, Styles of Description. Developing HDL code for logic circuits using Verilog HDL program. **VERILOG DATA FLOW DESCRIPTION:** Highlights of Data flow description, Structure of Data flow description.(Section 2.1 to 2.2 (only Verilog) of Text3) **Text Book**: Text 3: Chapter 1: 1.1 to 1.6.2, 1.6.4 Chapter 2: 2.1, 2.2 (only Verilog)	
Module-5	**7 Hours**
VERILOG BEHAVIORAL DESCRIPTION: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers (2:1, 4:1, 8:1). (Section 3.1 to 3.4 (only Verilog) of Text 3) **VERILOG STRUCTURAL DESCRIPTION**: Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder.(Section 4.1 to 4.2 of Text 3) **Text Book:** Text 3 – Chapter 3: 3.1 to 3.4, Chapter 4: 4.1, 4.2	
PRACTICAL COMPONENT OF IPCC (Experiments can be conducted either using any circuit simulation software) 1 To simplify the given Boolean expressions and realize using Verilog program 2 To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description. 3 To realize 4-bit ALU using Verilog Behavioral description. 4 To realize the following Code converters using Verilog Behavioral description a) Gray to binary and vice versa b) Binary to excess3 and vice versa 5 To realize using Verilog Behavioral description:8:1mux, 8:3 encoder, Priority encoder 6 To realize using Verilog Behavioral description:1:8 Demux, 3:8 decoder, 2 –bit Comparator 7 To realize using Verilog Behavioral description: Flip-flops: a) JK type b) SR type c) T type and d) D type 8 To realize Counters-up/down (BCD and binary) using Verilog Behavioral description. Demonstration Experiments: Use FPGA/CPLD kits for down loading Verilog codes and check the output for interfacing experiments. 9 Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified	

direction (by N steps).

10 Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Apply the knowledge of K Maps and Quine - McCluskey minimization technique for simplification of Boolean expressions. (PO – 1,2,3, PSO – 1,2)

CO2: Analyze and design for combinational logic circuits. (PO – 1,2,3, PSO – 1,2)

CO3: Analyze the concepts of Latches and Flip Flops (SR, D, T and JK) and to design the synchronous sequential circuits using Flip Flops. (PO – 1,2,3, PSO – 1,2)

CO4: Model Combinational circuits and sequential circuits using Dataflow descriptions. (PO – 1,2,3, PSO – 1,2)

CO5: Model Combinational circuits and sequential circuits using Behavioral, and Structural descriptions (PO – 1,2, PSO – 1)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests and **10 marks** for other assessment methods.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.

- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Textbook:

1. Digital Logic Applications and Design by John MYarbrough,Thomson Learning,2001.
2. Digital Principles and Design by Donald D Givone, McGraw Hill, 2002.
3. HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dream techpress.

Reference Books:

1. Fundamentals of Logic Design, Charles H. Roth (Jr.), West publications, 4th Edition, 1992, ISBN- 13: 978-0-314-92218-2.
2. Digital Fundamentals, Thomas Floyd, 11th Edition, Pearson Education India, ISBN 13: 978-1-292-07598-3, 2015.
3. Verilog HDL: A Guide to Digital Design & Synthesis, Samir Palnitkar, SunSoft Press, 1stEdition, 1996, ISBN: 978-81-775-8918-4.
4. Digital Logic and Computer Design, M. Morris Mano, Pearson Education Inc., 13th Impression, 2011, ISBN: 978-81-7758-409-7.

Web links and Video Lectures(e-Resources):

- http://acl.digimat.in/nptel/courses/video/117105080/L13.html
- **https://onlinecourses.nptel.ac.in/noc25_ee24/unit?unit=32&lesson=35**
- **https://onlinecourses.nptel.ac.in/noc25_ee24/unit?unit=47&lesson=48**

- **https://onlinecourses.nptel.ac.in/noc25_ee24/unit?unit=63&lesson=64**
- **https://onlinecourses.nptel.ac.in/noc25_ee24/unit?unit=70&lesson=71**
- **https://onlinecourses.nptel.ac.in/noc25_ee24/unit?unit=70&lesson=72**
- **https://onlinecourses.nptel.ac.in/noc25_ee24/unit?unit=41&lesson=42**
- http://acl.digimat.in/nptel/courses/video/117105080/L13.html

Virtual Lab Links:

- **https://dec-iitkgp.vlabs.ac.in/**

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Flipped classroom
- Assessment Methods for 10 Marks (opt two Learning Activities)
  - Quizzes
  - Assignment & online certifications
  - Use online simulator - https://www.multisim.com/ to work with digital circuits design
  - Learn TI CAD - https://www.ti.com/tool/TINA-TI or https://www.tina.com/ for simulation of analog and digital circuits

Applied Numerical Methods for EC Engineers			
Course Code	24EC36A	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	1:0:0	**SEE Marks**	50
Credits	03	**Total Marks**	100
Contact Hours	40	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Basic Mathematics

Course Objectives:

- To provide the knowledge and importance of error analysis in engineering problems
- To represent and solve an application problem using a system of linear equations
- Analyze regression data to choose the most appropriate model for a situation.
- Familiarize with the ways of solving complicated mathematical problems numerically
- Prepare to solve mathematical models represented by initial or boundary value problems

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching

Module-1	8 Hours

Errors in computations and Root of the equations: Approximations and Round Off -Errors in computation: Error definitions, Round-Offerrors, Truncation errors and the Taylor series-The Taylor series, Error Propagation, Total numerical error,Absolute,Relative and percentage errors,Blunders, Formulation errors and data uncertainty. Roots of equations: Simple fixed point iteration methods. Secant Method, Muller's method, and Graeffe's Roots Squaring Method. Aitkin's Method.

Module-2	8 Hours

Solution of System of Linear Equations: Rank of the matrix, Echelon form, Linearly dependent and independent equations, Solutions for linear equations, Partition method, Croute's Triangularisation method. Relaxation method. Solution of non-linear simultaneous equations by Newton-Raphson method. Eigen Values and properties, Eigen Vectors, Bounds on Eigen Values, Jacobi's method, Given's method for symmetric matrices.

Module-3	8 Hours

Curve Fitting: Least-Squares Regression: Linear Regressions, Polynomial regressions, Multiple Linear regressions, General Linear Least squares, Nonlinear Regressions, QR Factorization. Curve Fitting with Sinusoidal Functions Introduction to Splines,Linear Splines, Quadratic Splines, Cubic Splines. Bilinear Interpolation.

Module-4 **8 Hours**

Numerical integration, Difference equations and Boundary Value Problems: Romberg's method, Euler-Maclaurin formula, Gaussian integration for n = 2 and n=3. Numerical double integration by trapezoidal and Simpson's 1/3 rd rule. Solution of linear difference equations. Boundary-Value Problems, Introduction. The Shooting Method, Finite-Difference Methods

Module-5 **8 Hours**

Numerical solution of partial differential equations: Classifications of second-order partial differential equations,Finite difference approximations to partial derivatives. Solution of:Laplace equation, Poisson equations, one-dimensional heat equation and wave equations.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

CO1: Explain and measure errors in numerical computations (PO – 1,2)

CO2: Test for consistency and solve a system of linear equations. (PO – 1,2)

CO3: Construct a function which closely fits given n- n-points of an unknown function. (PO – 1,2)

CO4: Understand and apply the basic concepts related to solving problems by numerical differentiation and numerical integration. (PO – 1,2)

CO5: Use appropriate numerical methods to study phenomena modelled as partial differential equations. (PO – 1,2)

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE, the minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.Continuous internal Examination (CIE)

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is projectbased then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

The Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Textbook:

1. Steven C. Chapra & Raymond P. Canale: "Numerical Methods for Engineers and Scientists", McGraw Hill, 8th Edition, 2020.

2. Steven C. Chapra: "Applied Numerical Methods with MATLAB for Engineers and Scientists", McGraw Hill, Fifth Edition, 2023.

3. B. S. Grewal: "Numerical Methods in Engineering & Science with programs in C, C++ and MATLAB", Khanna Publishers, 10 h Ed., 2015.

Reference Books:

1.John H. Mathews & Kurtis D. Frank: "Numerical Methods Using MATLAB", PHI Publications, 4th Edition, 2005.

2.Won Young Yang, Wenwu Cao, Tae Sang Chung, John Morris: "Applied Numerical Methods Using MATLAB" , WILEY Interscience, Latest Edition, 2005.

Web links and Video Lectures(e-Resources):

- **http://nptel.ac.in/courses.php?disciplineID=111**
- **http://www.class-central.com/subject/math(MOOCs)**
- **http://academicearth.org/**
- **VTU e-Shikshana Program**
- **VTU EDUSAT Program.**

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Quizzes
- Assignments
- Seminar

COMPUTER ORGANIZATION AND ARCHITECTURE			
Course Code	24EC36B	**CIE Marks**	50
Teaching Hours/Week (L:T:P)	3:0:0	**SEE Marks**	50
Total Hours of Pedagogy	40	**Total Marks**	100
Credits	03	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Digital Logic Design
- Computer Architecture Basics
- Understanding of Algorithms
- Problem-Solving Skills

Course objectives: This course will enable students to:

- Explain the basic sub systems of a computer, their organization, structure and operation.
- Illustrate the concept of programs as sequences of machine instructions.
- Demonstrate different ways of communicating with I/O devices
- Describe memory hierarchy and concept of virtual memory.
- Illustrate organization of simple pipelined processor and other computing systems.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS(Higher order Thinking)questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
- Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.

Module-1 **8 Hours**

Basic Structure of Computers: Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Software, Performance -Processor Clock, Basic Performance Equation**(upto1.6.2ofChap1ofText).**

Machine Instructions and Programs: Numbers, Arithmetic Operations and Characters, IEEE standard for Floating point Numbers, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing **(up to 2.4.6 of Chap 2 and 6.7.1 of Chap 6 of Text).**

Module-2	**8 Hours**

Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions (from2.4.7ofChap2, except 2.9.3, 2.11 & 2.12 of Text).

Module-3	**8 Hours**

Input/ Output Organization: Accessing I/O Devices, Interrupts -Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Direct Memory Access (upto4.2.4and4.4except4.4.1ofChap4ofText).

Module-4	**8 Hours**

Memory System: Basic Concepts, Semiconductor RAM Memories-Internal organization of memory chips, Static memories, Asynchronous DRAMS, Read Only Memories, Cash Memories, Virtual Memories, Secondary Storage- Magnetic Hard Disks (5.1,5.2,5.2.1,5.2.2,5.2.3,5.3,5.5(except 5.5.1 to 5.5.4), 5.7 (except5.7.1), 5.9, 5.9.1 of Chap 5 **of Text).**

Module-5	**8 Hours**

Basic Processing Unit: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hardwired Control, Microprogrammed Control (up to 7.5 except 7.5.1 to7.5.6 of Chap 7 of Text).

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

CO1: Explain the basic organization of a computer system.(PO-

CO2: Describe the addressing modes, instruction formats and program control statement.

CO3: Explain different ways of accessing an input/ output device including interrupts.

CO4: Illustrate the organization of different types of semiconductor and other secondary storage memories.

CO5: Illustrate simple processor organization based on hard wired control and micro-programmed control.

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

Suggested Learning Resources:

Book

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5th Edition,Tata McGrawHill,2002.

ReferenceBooks:

2. David A. Patterson, John L. Hennessy: Computer Organization and Design-The Hardware/ Software InterfaceARM Edition, 4th Edition, Elsevier,2009.
3. William Stallings: Computer Organization &Architecture,7th Edition, PHI, 2006.
4. Vincent P. Heuring & Harry F. Jordan: Computer Systems Design and Architecture, 2nd Edition, Pearson Education, 2004.

Web links and Video Lectures (e-Resources):

- https://elearning.vtu.ac.in/esk/P3/econtent/18EC46/index.php
- https://www.youtube.com/watch?v=pA6K5NgWTow
- https://www.youtube.com/playlist?list=PLaKtTm3mCI2alKlTvvJE4KqSEFjU6phDn
- **https://digimat.in/nptel/courses/video/108105102/L23.html**

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Flipped classroom
- Assessment Methods for 25 Marks (opt two Learning Activities)
  - Case Studies
  - Gate Based Aptitude Test
  - Certification course

Electronic Devices			
Course Code	**24EC36C**	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	3:0:0	**SEE Marks**	50
Credits	03	**Total Marks**	100
Contact Hours	40	**Exam Hours**	03
Examination type (SEE)	Theory		

Prerequisites:

- Basics Semiconductor devices.
- Basics of doping and diffusion principles
- Basics of opto electronic devices

Course Objectives:

This course is intended to:

- Understand the basics of semiconductor physics and electronic devices.
- Describe the mathematical models BJTs and FETs along with the constructional details.
- Understand the construction and working principles of optoelectronic devices
- Understand the fabrication process of semiconductor devices and CMOS process integration.

Teaching-Learning Process (General Instructions):

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Problem based learning
4. Demonstration based Teaching

Module- 1 **8 Hours**

Semiconductors

Bonding forces in solids, Energy bands, Metals, Semiconductors and Insulators, Direct and Indirect semiconductors, Electrons and Holes, Intrinsic and Extrinsic materials, Conductivity and Mobility, Drift and Resistance, Effects of temperature and doping on mobility, Hall Effect. (Text 1: 3.1.1, 3.1.2, 3.1.3, 3.1.4, 3.2.1, 3.2.3, 3.2.4, 3.4.1, 3.4.2, 3.4.3, 3.4.5).

Module- 2 **8 Hours**

P-N Junctions

Forward and Reverse biased junctions- Qualitative description of Current flow at a junction, reverse

bias, Reverse bias breakdown- Zener breakdown, avalanche breakdown, Rectifiers. (Text 1: 5.3.1, 5.3.3, 5.4, 5.4.1, 5.4.2, 5.4.3)
Optoelectronic Devices Photodiodes: Current and Voltage in an Illuminated Junction, Solar Cells, Photodetectors. Light Emitting Diode: Light Emitting materials.(Text 1: 8.1.1, 8.1.2, 8.1.3, 8.2, 8.2.1

Module- 3 **8 Hours**

Bipolar Junction Transistor
Fundamentals of BJT operation, Amplification with BJTS, BJT Fabrication, The coupled Diode model (Ebers-Moll Model), Switching operation of a transistor, Cutoff, saturation, switching cycle, specifications, Drift in the base region, Base narrowing, Avalanche breakdown. (Text 1: 7.1, 7.2, 7.3, 7.5.1, 7.6, 7.7.1, 7.7.2, 7.7.3).

Module- 4 **8 Hours**

Field Effect Transistors
Basic pn JFET Operation, Equivalent Circuit and Frequency Limitations, MOSFET-Two terminal MOS structure- Energy band diagram, Ideal Capacitance – Voltage Characteristics and Frequency Effects, Basic MOSFET Operation- MOSFET structure, Current-Voltage Characteristics. (Text 2: 9.1.1, 9.4, 9.6.1, 9.6.2, 9.7.1, 9.7.2, 9.8.1, 9.8.2).

Module- 5 **8 Hours**

Fabrication of p-n junctions

Thermal Oxidation, Diffusion, Rapid Thermal Processing, Ion implantation, chemical vapour deposition, photolithography, Etching, metallization. (Text 1: 5.1) Integrated Circuits Background, Evolution of ICs, CMOS Process Integration, Integration of Other Circuit Elements. (Text 1: 9.1, 9.2, 9.3.1, 9.3.3).

Course outcomes (Course Skill Set):

At the end of the course, students will be able to:

CO1: Understand the principles of semiconductor Physics (PO-1,2,6)
CO2: Understand the principles and characteristics of different types of semiconductor devices (PO-1,2,6)
CO3: Understand the fabrication process of semiconductor devices (PO-1,2,3)
CO4: Utilize the mathematical models of semiconductor junctions for circuits and systems (PO-1,2,4)
CO5: Utilize the mathematical models of MOS transistor for circuits and systems (PO-1,4,5)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the regulations shall be considered; if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books:

1. Ben. G. Streetman, Sanjay Kumar Banergee, "Solid State Electronic Devices", 7thEdition, Pearson Education, 2016, ISBN 978-93-325-5508-2.
2. Donald A Neamen, Dhrubes Biswas, "Semiconductor Physics and Devices", 4th Edition,

MCGraw Hill Education, 2012, ISBN 978-0-07-107010-2

Reference Books:

1. S. M. Sze, Kwok K. Ng, “Physics of Semiconductor Devices”, 3rd Edition, Wiley, 2018.
2. A. Bar-Lev, “Semiconductor and Electronic Devices”, 3rd Edition, PHI, 1993.

Web links and Video Lectures (e-Resources):

https://www.youtube.com/watch?v=n9ZytPvXi7w
https://www.youtube.com/watch?v=oLu_sE9hwd8
http://kcl.digimat.in/nptel/courses/video/108106181/L25.html
https://digimat.in/nptel/courses/video/117103063/L31.html
http://www.digimat.in/nptel/courses/video/117106093/L34.html

Sensors and Instrumentation			
Course Code	24EC36D	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	3:0:0	**SEE Marks**	50
Credits	03	**Total Marks**	100
Contact Hours	40	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Basic Electrical
- Basic Electronics

Course Objectives:

- Understand various technologies associated in manufacturing of sensors
- Acquire knowledge about types of sensors used in modern digital systems
- Get acquainted about material properties required to make sensors
- Understand types of instrument errors and circuits for multirange Ammeters and Voltmeters.
- Describe principle of operation of digital measuring instruments and Bridges.
- Understand the operations of transducers and instrumentation amplifiers.

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Project based Teaching

Module-1 **8 Hours**

Introduction to sensor-based measurement systems:
General concepts and terminology, sensor classification, Primary Sensors- Temperature Sensors- Bimetal, Pressure sensors, Flow velocity and Flowrate sensors, Level sensors, acceleration and Inclination sensors, velocity sensors, material for sensors.

Text Book 1-1.1, 1.7-1.8

Module-2 **8 Hours**

Self-generating Sensors: Thermoelectric sensors-Thermocouples, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, Electrochemical sensors.

Text Book 1 :6.1.1, 6.1.3, 6.2.1, 6.2.2, 6.2.3, 6.3.1, 6.3.2, 6.3.3, 6.4.1,6.4.2,6.5

Module-3	8 Hours

Principles of Measurement: Static Characteristics, Error in Measurement, Types of Static Error. Multirange Ammeters, Multirange voltmeter.

Text Book 1.2-1.6, 2:3.2,4.4

Digital Voltmeter: Ramp Technique, Dual slope integrating Type DVM, Direct Compensation type and Successive Approximations type DVM

Text Book 2: 5.1-5.3, 5.5,5.6)

Module-4	8 Hours

Digital Multimeter: Digital Frequency Meter and Digital Measurement of Time, Function Generator, Digital storage Oscilloscope.

Bridges: Measurement of resistance: Wheatstone's Bridge, AC Bridges – Anderson Bridg, Capacitance and Inductance Comparison bridge, Wien's bridge.

Text Book 2: refer 6.2,6.3 up to 6.3.2, 6.4 up to 6.4.2, 8.8,8.32, 11.2, 11.8 -11.10, 11.14.

Module-5	8 Hours

Transducers: Introduction, Electrical Transducer, Resistive Transducer, Resistive position Transducer, Resistance Wire Strain Gauges, Resistance Thermometer, Thermistor, LVDT.

Text Book 2:13.1-13.3,13.5, 13.6 up to 13.6.1,13.7,13.8,13.11.

Instrumentation Amplifier using Transducer Bridge, Temperature indicators using Thermometer, Light Intensity meter Analog Weight Scale

Text Book 2:14.3.3, 14.4.1,14.4.2, 14.4.3.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Understand the Fundamental Concepts of Sensors and Measurement Systems. (PO – 1,2,3, PSO – 1,3)
CO2: Demonstrate Knowledge of Self-Generating Sensors and Their Applications. (PO – 1,2,3, PSO – 1,3)
CO3: Apply Principles of Measurement and Error Analysis in Sensor Systems. (PO – 1,2,3, PSO – 1,3)
CO4: Gain Proficiency in the Use of Bridges and Digital Measurement Instruments.(PO –1,2,3, PSO – 1,3)
CO5: Analyze Sensor-Based Transducer Systems for Measurement Applications. (PO – 1,2,3, PSO – 1,3)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/

course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the regulations; if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Textbook:

1. "Sensors and Signal Conditioning", Ramon Pallas Areny, John G. Webster,2nd edition, John Wiley and Sons,2000
2. H.S.Kalsi, "Electronic Instrumentation", Mc Graw Hill,3rd Edition and 4th Edition,2012, ISBN:9780070702066.

Reference Books:

1. DavidA. Bell, "Electronic Instrumentation & Measurements", Oxford University Press PHI 2ndEdition, 2006, ISBN 81-203-2360-2.
2. D. Helfrick and W.D. Cooper, "Modern Electronic Instrumentation and Measuring Techniques", Pearson, 1stEdition, 2015, ISBN: 9789332556065.

Web links and Video Lectures(e-Resources):

- https://www.youtube.com/watch?v=9EsOFiP1J2E
- https://www.youtube.com/watch?v=hdaVgptDQAc
- https://www.youtube.com/watch?v=HY39LA6H-Lo
- https://www.youtube.com/watch?v=c-Ioo_Q9__Q
- https://www.youtube.com/watch?v=GR8WywKMiiQ
- https://www.youtube.com/watch?v=zkixSsT2p7w
- https://www.youtube.com/watch?v=nar2I82bJvU

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Flipped classroom
- Assessment Methods for 25 Marks (opt two Learning Activities)
  - Quiz
  - Assignment
  - MOOC Assignment for selected Module

LABVIEW Programming			
Course Code	24EC37A	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	0:0:2	**SEE Marks**	50
Credits	01	**Total Marks**	100
Contact Hours	12	**Exam Hours**	3
Examination type (SEE)	Practical		

Prerequisites:

The students should have knowledge on

- Basic Programming Skills
- Familiarity with Computers and Software
- LabVIEW Software Installed
- Basic Knowledge of Electronics
- Block Diagram Logic

Course objectives:

- Aware of various front panel controls and indicators.
- Connect and manipulate nodes and wires in the block diagram.
- Locate various tool bars and pull-down menus for the purpose of implementing specific functions.
- Locate and utilize the context help window.
- Familiar with LabVIEW and different applications using it.

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Demonstration based Teaching

Sl.NO	VI Programs(using LabVIEW software)to realize the following:
1	Basic arithmetic operations: addition, subtraction, multiplication and division
2	Boolean operations: AND, OR, XOR, NOT and NAND
3	Sum of ‘n’ numbers using ‘for’ loop
4	Factorial of a given number using ‘for’ and ‘while’ loop
5	Bundle and Unbundle Cluster.
6	Display random number 0 to 5 into 3 different charts (strip, slope,sweep).
7	Sorting even numbers using ‘while’ loop in an array
8	Finding the array maximum and array minimum
9	Build a Virtual Instrument that simulates a heating and cooling system. The system must be able to be controlled manually or automatically.

10	Build a Virtual Instrument that simulates a Basic Calculator (using formula node).
11	Build a Virtual Instrument that simulates a Water Level Detector.
12	Demonstrate how to create a basic VI which calculates the area and perimeter of a circle.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

CO1:Use LabVIEW to create data acquisition, analysis and display operations
CO2:Create user interfaces with charts, graph and buttons
CO3:Use the programming structures and data types that exist in LabVIEW
CO4:Use various editing and debugging techniques.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%,

Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. Virtual Instrumentation using LABVIEW, Jovitha Jerome,PHI,2011
2. Virtual Instrumentation using LABVIEW, Sanjay Gupta, Joseph John, TMH, Mc Graw Hill, Second Edition,2011.

Web links and Video Lectures(e-Resources):

1. https://youtu.be/G47Q_8HVBk4?feature=shared
2. https://youtu.be/Lrf2LJmWDkQ?feature=shared

Virtual Lab Links:

- **https://www.ni.com/en-us/innovations/virtual-labs.html**

BASICS OF EMBEDDED C			
Course Code	24EC37B	**CIE Marks**	50
Teaching Hours/Week (L:T:P)	0:0:2	**SEE Marks**	50
Total hours of Pedagogy	12	**Total Marks**	100
Credits	01	**Exam Hours**	03
Examination type (SEE)	Practical		

Pre-requisite:
Basic knowledge of programming and electronic devices is recommended.

Course objectives: This course will enable students to:

- Understand the basic programming of Microprocessor and microcontroller.
- Develop the microcontroller-based programs for various application in simulation environment
- Program a microcontroller to control an external hardware using suitable I/O ports.

Conduct the following experiments by writing C Program using Keil microvision simulator/any suitable simulator (any 8051/PIC18 /PIC16 microcontroller can be chosen as the target).

SL. No	List of Experiments
1.	Write a program to multiply two 16 bit binary numbers.
2.	Write a program to find the sum of first 10 integer numbers.
3.	Write a program to find factorial of a given number
4.	Write a program to add an array of 16bit numbers and store the 32 bit result in internal RAM
5.	Write program to find the square of a number (1to10) using look-up table.
6.	Write a program to find the largest/smallest number in an array of 32 numbers
7.	Write a program to arrange a series of 32bit numbers in ascending/descending order
8.	Write a program to count the number of ones and zeros in two consecutive memory locations.
9.	Write a program to scan a series of 32bit numbers to find how many are negative
10.	Write a program to display “Hello World” message (either in simulation mode or interface an LCD display).
11.	Write a program to generate the waveforms: square, triangle and ramp, using any processor.
12.	Write a program to run a stepper motor in clock wise and counter clockwise direction with a given step angle.

Course outcomes (Course Skill Set):
At the end of the course the student will be able to:

CO1: Apply Embedded C programming skills to perform arithmetic and logical operations on 8-bit and 16-bit data using suitable Microcontroller.(PO – 1,2,3, PSO – 1,3)
CO2: Develop Embedded C programs using decision-making and looping statements for basic control operations.(PO – 1,2,3, PSO – 1,3)
CO3: Develop testing and experimental procedures on suitable Microcontroller, analyze their operation under different cases.(PO – 1,2,3, PSO – 1,3)
CO4: Interface peripheral devices such as LCD, stepper motor, and digital-to-analog converter (DAC) with suitable microcontroller using Embedded C programs. (PO – 1,2,3, PSO – 1,3)
CO5: Design and create Mini projects.(PO – 1,2,3, PSO – 1,3)

Assessment Details (both CIE and SEE)

- The weight-age of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.
- The minimum passing mark for the CIE is 40% of the maximum marks (20 marks).
- A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course.
- The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation :

CIE marks for the practical course is 50 Marks.

The split-up of CIE marks for record/ journal and test are in the ratio 60:40.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weight-age to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 50 marks, the first test shall be conducted after the 5^{th} week of the semester and the second test shall be conducted after the 10^{th} week of the semester.

- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The average of 02 tests is scaled down to 20 marks (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester-End Examination :

SEE marks for the practical course is 50 Marks. SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

1. All laboratory experiments are to be included for practical examination.
2. (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.
3. Students can pick one question (experiment) from the questions prepared by the internal /external examiners jointly.
4. Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
5. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks.
6. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
7. Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero. The duration of SEE is 03 hours.

Suggested Learning Resources:

Textbook:

1. "The 8051Microcontroller: Hardware, Software and Applications", V Udaya Shankara and M S Mallikarjuna Swamy, McGraw Hill Education, First edition, 2017.

Reference Books:

1. "Practical Embedded Computing: A hands on Introduction to ARM Microcontrollers", Dr Dinesh Murugan and Hani Ahmad Assi, Microchip Technology, First Edition 2025.

Web links and Video Lectures(e-Resources):

- https://elearning.vtu.ac.in/esk/P3/econtent/18EC46/index.php
- https://www.youtube.com/watch?v=pA6K5NgWTow

- https://www.youtube.com/playlist?list=PLaKtTm3mCI2alKlTvvJE4KqSEFjU6phDn
- **https://digimat.in/nptel/courses/video/108105102/L23.html**

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Flipped classroom
- Assessment Methods for 25 Marks (opt two Learning Activities)
    - Case Studies
    - Programming Assignment
    - Gate Based Aptitude Test
    - Certification course

PCB Design			
Course Code	24EC37C	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	1:0:0	**SEE Marks**	50
Credits	01	**Total Marks**	100
Contact Hours	15	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Basic Electrical
- Basic Electronics

Course Objectives:

- Students are able to design an electronic printed circuit board for a specific application
- Understand industry standard software Tools for PCB design
- Able to understand the procedural steps of developing circuit schematic, board files, image transferring, assembly, soldering and testing.

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Project based Teaching

Module-1	**3 Hours**

Introduction: What is PCB. Advantages and Disadvantages of PCB , Components of PCB , Electronic components, ,Microprocessors and Microcontrollers, IC's , Surface Mount Devices (SMD) Classification of PCB , Single, double, multilayer and flexible boards , Manufacturing of PCB , PCB standards

Module-2	**3 Hours**

Schematic diagram of PCB: General, Mechanical and Electrical design considerations of PCB , Placing and Mounting of components in PCB , Conductor spacing and routing guidelines , Heat sinks and package density of PCB ,Net list , Creating components for library, Tracks, Pads, Vias , Power plane and grounding of PCB

Module-3	**3 Hours**

Design automation: Design Rule Checking b. Class Test, Exporting Drill and Gerber Files, Footprints and Libraries Adding and Editing Pins. Copper clad laminates materials, Electrical & Physical Properties of laminates, Types of laminates, Soldering techniques, Image transfer.

Module-4 **3 Hours**

Photo printing, Screen Printing, Film master preparation, Plating techniques, Etching techniques, Lead cutting.

Module-5 **3 Hours**

Soldering Techniques, Testing of PCB, Quality controls of PCB, Trends in PCB Industries, Environmental concerns in PCB industry, Class Test

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

CO1: Familiarize with the type of devices/components that may be mounted on PCB(PO – 1,2,3,5 PSO – 1,3)

CO2: Understand the PCB layout techniques for optimized component density and power saving. (PO – 1,2,3,5 PSO – 1,3)

CO3: Perform design and printing of PCB with the help of various image transfer and soldering techniques(PO – 1,2,3,5 PSO – 1,3)

CO4: Understand the trends in the current PCB industry(PO – 1,2,3,5 PSO – 1,3)

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous internal Examination (CIE)

For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.

The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered

Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.

For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examinations (SEE)

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is **01 hour.** The student has to secure a minimum of 35% of the maximum marks meant for SEE.

Suggested Learning Resources:

Textbook:

1. Printed Circuit Board – Design, Fabrication, Assembly & Testing, R.S. Khandpur, Tata McGraw Hill Publisher

2. Printed circuit Board – Design & Technology, Walter C. Bosshart, Tata McGraw Hill

Open Source Tools: Tinker CAD

Web links and Video Lectures(e-Resources):

- **https://www.youtube.com/playlist?list=PL3aaAq2OJU5EsYtNwTPHNO3RHNJN34FbO**
- **https://www.youtube.com/watch?v=OGq5RIYf30Y**

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

PCB design using software Tinker CAD

MATLAB Programming			
Course Code	24EC37D	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	1:0:0	**SEE Marks**	50
Credits	01	**Total Marks**	100
Contact Hours	15	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Basic Programming

Course Objectives:

- Understand the MATLAB commands and functions.
- Create and Execute the script and function files
- Work with built in function, saving and loading data and create plots.
- Work with the arrays, matrices, symbolic computations, files and directories.
- Learn MATLAB programming with script, functions and language specific features.

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Project based Teaching

Module-1 **3 Hours**

Introduction: Basics of MATLAB, Simple arithmetic calculations, Creating and working with arrays and numbers.

Module-2 **3 Hours**

Creating and printing simple plots, Creating, saving and executing a script file, Creating and executing a function file, Working with arrays and matrices.

Module-3 **3 Hours**

Working with anonymous functions, Symbolic Computations, Importing and exporting data, Working with files and directories.

Module-4 **3 Hours**

Interactive computations: Matrices and vectors, Matrix and array operations, Character strings, Command line functions, Built-in functions, Saving and loading data, Plotting simple plots.

Module-5	3 Hours
Programming in MATLAB: Script Files, Function Files, Language specific Features.	

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

CO1: Use the syntax of MATLAB for arithmetic computations, arrays, matrices. (PO – 1,2,3, PSO – 1,3)

CO2: Use the built in function, saving and loading data, and create plots(PO – 1,2,3, PSO – 1,3)

CO3; Create program using symbolic computations, Importing and exporting data and files(PO – 1,2,3, PSO – 1,3)

CO4: Create program using character strings, Command line functions and Built-in functions. (PO – 1,2,3, PSO – 1,3)

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

Continuous internal Examination (CIE)

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examinations (SEE)

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is **01 hour.** The student has to secure a minimum of 35% of the maximum marks meant for SEE.

Suggested Learning Resources:

Textbook:

1. " Rudra Pratap, Getting Started with MATLAB – A quick Introduction for scientists and Engineers, Oxford University Press, 2010.

Web links and Video Lectures(e-Resources):

- https://www.youtube.com/watch?v=O41BWhXFu8E
- https://www.youtube.com/watch?v=EtUCgn3T9eE

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

MATLAB Programming

Principles of Communication Systems			
Course Code	24EC41	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	3:0:0:0	**SEE Marks**	50
Credits	03	**Total Marks**	100
Contact Hours	40	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge of

- Basic signal operations, Trigonometric identities
- Fourier Series Fourier Transform & Hilbert Transforms
- Probability and random process
- Oscillators, mixers, amplifiers, Filters

Course Objectives: This course will enable students to

- Understand and analyse concepts of Analog Modulation schemes viz; AM, FM., Low pass sampling and Quantization as a random process.
- Understand and analyse concepts digitization of signals viz; sampling, quantizing and encoding.
- Evolve the concept of SNR in the presence of channel induced noise and study Demodulation of analog modulated signals.
- Evolve the concept of quantization noise for sampled and encoded signals and study the concepts of
- reconstruction from these samples at a receiver.

Teaching-Learning Process (General Instructions)

Teachers can use the following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Demonstration based Teaching

Module-1 **8 Hours**

AMPLITUDE MODULATION: Introduction, Amplitude Modulation: Time & Frequency Domain Description, Switching modulator, Envelop detector.

DOUBLE SIDE BAND-SUPPRESSED CARRIER MODULATION: Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing.

SINGLE SIDE–BAND AND VESTIGIAL SIDEBAND METHODS OF MODULATION: SSB Modulation, VSB Modulation, Frequency Translation, Frequency Division Multiplexing, Theme Example: VSB Transmission of Analog and Digital Television. [Text1: 3.1 to 3.8]

Module-2 **8 Hours**

ANGLE MODULATION: Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM, Transmission bandwidth of FM Signals, Generation of FM Signals, Demodulation of FM Signals, FM Stereo Multiplexing, Phase–Locked Loop: Nonlinear model of PLL, Linear model of PLL, Nonlinear Effects in FM Systems. The Superheterodyne Receiver [Text1: 4.1 to 4.6]

Module-3 **8 Hours**

NOISE: Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth, Noise Figure.
NOISE IN ANALOG MODULATION: Introduction, Receiver Model, Noise in DSB-SC receivers. Noise in AM receivers, Threshold effect, Noise in FM receivers, Capture effect, FM threshold effect, FM threshold reduction, Pre-emphasis and De-emphasis in FM (Text1: 5.10, 6.1 to 6.6)

Module-4 **8 Hours**

SAMPLING AND QUANTIZATION: Introduction, Why Digitize Analog Sources? The Low pass Sampling process Pulse Amplitude Modulation. Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves. (Text1: 7.1 to 7.7)

Module-5 **8 Hours**

SAMPLING AND QUANTIZATION (Contd): The Quantization Random Process, Quantization Noise, Pulse–Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding, Filtering, Multiplexing; Delta Modulation (Text1: 7.8 to 7.10)

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

CO1: Understand the amplitude and frequency modulation techniques and perform time and frequency domain transformations. (PO – 1,2,3, PSO – 1,2,3)

CO2: Identify the schemes for amplitude and frequency modulation and demodulation of analog signals and compare the performance. (PO – 1,2,3, PSO – 1,2,3)

CO3: Characterize the influence of channel noise on analog modulated signals. (PO – 1,2,3, PSO – 1,2,3)

CO4: Understand the characteristics of pulse amplitude modulation, pulse position modulation and pulse code modulation systems. (PO – 1,2,3, PSO – 1,2,3)

CO5: Analyze and apply the fundamental concepts of quantization and random processes in digital communication systems. (PO – 1,2,3, PSO – 1,2,3)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE the minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the regulations; if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Textbook:

1. Simon Haykins & Moher, Communication Systems, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.

Reference Books:

1. B P Lathi and Zhi Ding, Modern Digital and Analog Communication Systems, Oxford University Press., 4th edition, 2010, ISBN: 97801980738002.
2. Simon Haykins, An Introduction to Analog and Digital Communication, John Wiley India Pvt. Ltd., 2008, ISBN 978–81–265–3653–5.
3. H Taub & D L Schilling, Principles of Communication Systems, TMH,2011

Web links and Video Lectures(e-Resources):

- https://www.youtube.com/watch?v=wqTv6jdUPL4&list=PLgwJf8NK-2e6MAucGEgjFqC3YtnZzsrTM
- https://www.youtube.com/watch?v=6Y9n8dMYL-o
- https://www.youtube.com/results?search_query=noise+in+communication+system
- https://www.youtube.com/watch?v=Uzwp2n4BZsg
- https://www.youtube.com/watch?v=ojPJeEnY5oo

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Assessment Methods for 25 Marks (opt two Learning Activities)
  - Simulation of modulation schemes using MATLAB
  - Quiz
  - MOOC/NPTEL certificate

Basic Signal Processing			
Course Code	24EC42	**CIE Marks**	50
Teaching Hours/Week (L:T:P)	3:0:0	**SEE Marks**	50
Credits	03	**Total Marks**	100
Contact Hours	40	**Exam Hours**	03
Examination Type	Theory		

Prerequisites

Knowledge of basic mathematics such as continuous function, discrete function & difference equations.

Course Objectives:

At the end of the course, students will be able to understand:

- Definition, classification and various operations on signals.
- Definition, properties and interconnection of systems.
- Representation of systems using impulse response and difference equations.
- Fourier representation of signals and systems.
- Importance of Z-transform and its significance in the analysis of systems.

Teaching-Learning Process

These are sample strategies, which teacher can use to accelerate the attainment of the various course outcomes and make Teaching–Learning more effective.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show video/animation films to explain the various operations in signals.
3. Adopt Problem Based Learning (PBL), which fosters student's analytical skills and develops thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
4. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
5. Discuss how every concept can be applied to the real world and when that's possible, it helps to improve the student's understanding.

Syllabus

Module -1 (8 Hours)

Signals: Definitions of a signalwith real-life examples, Continuous-time Vs Discrete-time signals, Elementary discrete-time signals, Sampling theorem (No proof), Operations on discrete-time signals, Classification of discrete-time signals, Numerical problems.
(Text Book T1).

Module -2 (8 Hours)

Systems: Definitions of a system with real-life examples, Properties of systems (Linear Vs Non-linear, Time-invariant Vs Time-variant, Memoryless Vs Not-memoryless, Causal Vs Non-causal, Stable Vs Unstable and Invertible Vs Non-invertible systems), System viewed as interconnection of operations, Numerical problems. (Text Book T1).

Module -3 (8 Hours)

Time domain representations of discrete-time LTI Systems: Impulse Response representation for discrete-time LTI systems, Properties of the impulse response of representation for discrete-time LTI systems (Commutative, Distributive, Associative, Memoryless, Causal, Stable and Invertibility), The unit step response of discrete-time LTI systems Difference equation representations for LTI systems and its solution, Numerical problems.
(Text Book T1).

Module -4 (8 Hours)

Fourier Representation of Discrete-Time Periodic Signals: Introduction to DTFS, definition, properties (No derivation) and basic problems (inverse Fourier series is excluded), Numerical problems.
FourierRepresentation of Discrete-Time Non-periodic Signals: Introduction to DTFT, definition,

DTFT of standard discrete-time signals andproperties, Numerical problems.
Applications of FourierRepresentations: Frequency Response of discrete-time LTI systems, Solution of difference equations, Numerical problems.
(Text Book T1).

Module -5 (8 Hours)

Z – Transform: Introduction,The Z-transform, Properties of Region of Convergence, Properties of Z-transform, Inverse Z-transform, Transform analysis of discrete-time LTI systems, The Unilateral Z-transform, Numerical problems.
(Text Book T1).

Course Outcomes:
This course will enable students to:

- Understand the mathematical description of continuous and discrete time signals and systems.
- Analyze the discrete time signals in time domain using convolution & difference equations
- Classify discrete-time signals into different categories based on their properties.
- Analyze discrete-time Linear Time Invariant (LTI) systems in time and transform domains.
- Build basics for understanding of courses such as signal processing, control system and communication.

Question paper pattern:

- The question paper will have ten questions.
- Each full Question consisting of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Suggested Learning Resources

Text Book:

T1: Simon Haykins and Barry Van Veen, "Signals and Systems", 2nd Edition, 2008, Wiley India. ISBN 9971-51-239-4.

Reference Books:

1. **Alan V Oppenheim, Alan S, Willsky and A Hamid Nawab,** "Signals and Systems" Pearson Education Asia / PHI, 2nd edition, 1997. Indian Reprint 2002.
2. **Michael Roberts,** "Fundamentals of Signals & Systems", 2nd edition, Tata McGraw-Hill, 2010, ISBN 978-0-07-070221-9.
3. **H. P Hsu, R. Ranjan,** "Signals and Systems", Schuam"s outlines, TMH, 2006.
4. **B. P. Lathi,** "Linear Systems and Signals", Oxford University Press, 2005.

Web links and Video Lectures (e-Resources):

(1) https://ocw.mit.edu
(2) NPTEL :: Electrical Engineering - NOC:Signals and Systems

Activity Based Learning: Programming Assignments (MATLAB) / Simulation can be given to improve programming skills. Quiz can conducted.

Electromagnetic Theory			
Course Code	24EC43	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	3:0:0	**SEE Marks**	50
Credits	03	**Total Marks**	100
Contact Hours	40	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on vector calculus

Course Objectives:

- Understand the applications of Coulomb's law and Gauss law to different charge distributions
- Study the physical significance of Divergence, Curl and Gradient.
- Understand the applications of Laplace's and Poisson's Equations to solve real time problems on capacitance of different charge distributions.
- Understand the physical significance of Biot-Savart's, Ampere's Law and Stokes' theorem for different current distributions.
- Infer the effects of magnetic forces, materials and inductance.
- Know the physical interpretation of Maxwell's equations and applications for Plane waves for their behavior in different media.
- Acquire knowledge of Poynting theorem and its application of power flow

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk
2. Power point presentation
3. ICT tools

Module-1 **8 Hours**

Coulomb's Law, Electric Field Intensity and Flux density

Coulomb's Law, Electric Field Intensity and Flux density: Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge distribution, Field of a line charge, Field due to Sheet of charge, Electric flux density, Numerical Problems.

Text book: Chapter 2.1 to 2.5, 3.1

Module-2 **8 Hours**

Gauss's law and Divergence: Gauss law, Application of Gauss law , Point form of Gauss law, Divergence, Maxwell's First equation ,Vector Operator ∇ and divergence theorem, Numerical Problems

Text book: Chapter 3.2 to 3.7

Energy, Potential and Conductors: Energy expended or work dme in moving a point charge in an electric field, The line integral, Current and Current density, Continuity of current.

Text book: Chapter 4.1 and 4.2, 5.1, 5.2

Module-3 **8 Hours**

Poisson's and Laplace's Equations: Derivation of Poisson's and Laplace's Equations, Uniqueness theorem. Examples of the solution of Laplace's equation, Numerical problems on Laplace equation

Text book: Chapter 7.1to 7.3

Steady Magnetic Field: Biot-Savart Law, Ampere's circuital law, Curl, Stokes' theorem, Magnetic flux and magnetic flux density

Text book: Chapter 8.1to 8.5

Module-4 **8 Hours**

Magnetic Forces: Force on a moving charge, differential current elements, Force between differential current elements, Numerical problems

Text book: Chapter 9.1 to 9.3

Magnetic Materials: Magnetization and permeability, Magnetic boundary conditions, The magnetic circuit, Numerical problems

Text book : Chapter 9.6 to 9.8

Module-5 **8 Hours**

Faraday' law of Electromagnetic Induction – Faraday's law, displacement current, Maxwell's equations in point form, and integral form, Numerical problems

Text book: Chapter 10.1 to 10.4

Uniform Plane Wave: Wave propagation in free space, Wave propagation in good conductor, Skin effect or Depth of penetration Poynting's theorem and wave power, Numerical problems**.**

Text book: Chapter 12.1,12.3,12.4

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Determine electrostatic force, electric field due to point, linear, volume charges by applying conventional methods and charge in a volume.(PO-1,PO-2,PSO-1,PSO-2)
CO2: Apply Gauss law to evaluate Electric fields due to different charge distributions and Volume Charge distribution .(PO-1,PO-2,PSO-1,PSO-2)
CO3: Determine potential and energy with respect to point charge and capacitance using Laplace equation and apply Biot-Savart's and Ampere's laws for evaluating Magnetic field for different current configurations.(PO-1,PO-2,PSO-1,PSO-2)
CO4: Evaluate magnetic force, potential energy and Magnetization with respect to magnetic materials and voltage induced in electric circuits .(PO-1,PO-2,PSO-1,PSO-2)
CO5: Apply Maxwell's equations for time varying fields, EM waves in free space and conductors and evaluate power associated with EM waves using Poynting theorem.(PO-1,PO-2,PO-3,PSO-1,PSO-2)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the regulations; if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.

3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Textbook:

1. W.H. Hayt and J.A. Buck, ―Engineering Electromagnetics, 8th Edition, Tata McGraw- Hill, 2014, ISBN-978-93-392-0327-6.

Reference Books:

1. Elements of Electromagnetics – Matthew N.O., Sadiku, Oxford University press, 4thEdn.
2. Electromagnetic Waves and Radiating systems – E. C. Jordan and K.G. Balman, PHI, 2ndEdn.
3. Electromagnetics- Joseph Edminister, Schaum Outline Series, McGraw Hill.
4. N. Narayana Rao, - Fundamentals of Electromagnetics for Engineering, Pearson

Web links and Video Lectures(e-Resources):

- https://youtu.be/pGdr9WLto4A?feature=shared
- https://www.youtube.com/watch?v=eXpy5hQpA2Q
- https://youtu.be/0A45kt2U3U8?feature=shared
- https://youtu.be/yBCTLNZ6fdE?feature=shared
- https://youtu.be/U9LDcmKUGS0?feature=shared
- https://youtu.be/ntWKMkXAuDA?feature=shared
- https://youtu.be/QPw4GYz5Unc?feature=shared
- https://youtu.be/aYRBXI63Oqk?feature=shared
- https://youtu.be/deI8cJiCKEo?feature=shared
- https://youtu.be/ibF0L6X53tg?feature=shared
- https://youtu.be/uC1W_1eyjPk?feature=shared

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Flipped classroom
- Quiz

CONTROL SYSTEMS			
Course Code	**24EC44**	**CIE Marks**	50
Teaching Hours/Week (L:T:P)	(3:0:2)	**SEE Marks**	50
Credits	4	**Total Marks**	100
Contact Hours	55	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Kirchhoff's Voltage Law (KVL)
- Kirchhoff's Current Law (KCL)
- Laplace Transform
- Basic knowledge of matrix and determinants formulas

Course Objectives:

- Understand basics of control systems and design mathematical models using block diagram reduction, SFG, etc.
- Understand Time domain and Frequency domain analysis.
- Analyze the stability of a system from the transfer function
- Familiarize with the State Space Model of the system.

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with BlackBoard
2. ICT based Teaching
3. Demonstration based Teaching

Module-1	**11 Hours**

Introduction to Control Systems: Types of Control Systems, Effect of Feedback Systems, Differential equation of Physical Systems -Mechanical Systems, Electrical Systems, Analogous Systems. (Textbook 1: Chapter 1.1, 2.2)

Module-2	**11 Hours**

Block diagrams and signal flow graphs: Transfer functions, Block diagram algebra and Signal Flow graphs. (Textbook 1: Chapter 2.4, 2.5, 2.6)

Module-3	**11 Hours**

Time Response of feedback control systems: Standard test signals, Unit step response of First and Second order Systems. Time response specifications, Time response specifications of second order

systems, steady state errors and error constants. Introduction to PI,PD and PID controller (Textbook 1: Chapter 5.3, 5.4, 5.5)

Module-4 **11 Hours**

Stability analysis: Concepts of stability, Necessary conditions for Stability, Routh stability criterion, Relative stability analysis: more on the Routh stability criterion.

Introduction to Root-Locus Techniques, The root locus concepts, Construction of root loci. (Textbook 1: Chapter 6.1, 6.2, 6.4, 6.5, 7.1, 7.2, 7.3)

Module-5 **11 Hours**

Frequency domain analysis and stability: Correlation between time and frequency response, Bode Plots, Experimental determination of transfer function. (Textbook 1: Chapter 4: 8.1, 8.2, 8.4) Mathematical preliminaries, Nyquist Stability criterion, (Stability criteria related to polar plots are excluded) (Textbook 1: 9.2, 9.3)

State Variable Analysis: Introduction to state variable analysis: Concepts of state, state variable and state models. State model for Linear continuous –Time systems, solution of state equations. (Textbook 1: 12.2, 12.3, 12.6)

Courseoutcomes(CourseSkillSet):

At the end of the course, the student will be able to:

CO1: Understand basics of control systems and Mathematical modeling (transfer function) of simple electrical, mechanical and electromechanical control . (PO – 1,2,3, PSO – 1,3)

CO2: The block diagram reduction and Signal flow graph analysis. . (PO – 1,2,3, PSO – 1,3)

CO3: Describe quantitative analysis of transient response of first and second order systems. . (PO – 1,2,3, PSO – 1,3)

CO4: Compute the RH criteria, Root to check the stability of the systems. . (PO – 1,2,3, PSO – 1,3)

CO5: Compute the Bode plot and Nyquist criteria to check the stability of the systems. Familiarize with the State Space Model of the system. . (PO – 1,2,3, PSO – 1,3)

PRACTICAL COMPONENT OF IPCC Using suitable simulation software (P-Spice/ MATLAB / Python / Scilab / OCTAVE / LabVIEW) demonstrate the operation of the following circuits:

Sl.No	Experiments
1	Implement Block diagram reduction technique to obtain transfer function a control system.
2	Implement Signal Flow graph to obtain transfer function a control system.
3	Simulation of poles and zeros of a transfer function.
4	Implement time response specification of a second order Under damped System, for different damping factors.
5.	Implement frequency response of a second order System.
6	Analyze the stability of the given system using Routh stability criterion.
7	Analyze the stability of the given system using Root locus.
8	Analyze the stability of the given system using Bode plots.
9	Analyze the stability of the given system using Nyquist plot.
10	Obtain the time response from state model of a system

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation for the component of IPCC

Two Tests each of 20 Marks (duration 01 hour)

- First test at the end of 5th week of the semester
- Second test at the end of the 10th week of the semester

Two assignments each of 10 Marks

- First assignment at the end of 4th week of the semester
- Second assignment at the end of 9th week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for 30 marks.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The 15 marks are for conducting the experiment and preparation of the laboratory record, the other 05 marks shall be for the test conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test (duration 03 hours) at the end of the 15th week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for 20 marks.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured out of 100 shall be reduced proportionally to 50

Suggested Learning Resources:

Suggested Learning Resources:

Text Books

1. Control Systems Engineering, I J Nagrath, M. Gopal, New age international Publishers, Fifth edition.

Reference Books

1. Morden Control System, K. Ogata, Pearson Education Asia/PHI, 4th Edition 2002
2. Automatic Control Systems, Benjamin C. Kuo, John Wiley India Pvt. Ltd, 8th Edition 2008
3. Feedback and Control Systems, Joseph J Distefano III et.al., Schaum's Outlines,TMH, 2th Edition 2007

Web links and Video Lectures(e-Resources):

- https://www.youtube.com/watch?v=XMfH2P2Fc6Q
- https://www.youtube.com/watch?v=ZAoIhtZsRX8
- https://www.youtube.com/watch?v=Vvg29q1E2YA
- https://www.youtube.com/watch?v=My1O02wi1AA
- https://www.youtube.com/watch?v=GvNW3fBy7CU
- https://www.youtube.com/watch?v=mWFuINeMpnk
- https://www.youtube.com/watch?v=uCm4n897cOY
- https://www.youtube.com/watch?v=T8ATyg_Fo6Y
- https://www.youtube.com/watch?v=dAwCtTPX2XM
- https://www.youtube.com/watch?v=O-ZMhu-aEwI
- https://www.youtube.com/watch?v=gR5nDxw5lds

- https://www.youtube.com/watch?v=OYPXiC7QjUM
- https://www.youtube.com/watch?v=t1BrHAYhvog
- https://www.youtube.com/watch?v=MRyICw3eOJs
- https://www.youtube.com/watch?v=o3bRqh4IlCA
- https://www.youtube.com/watch?v=ww9rHEAwTnE
- https://www.youtube.com/watch?v=psx3gsKbY2U
- https://www.youtube.com/watch?v=qJXoZ2AE_bI
- https://www.youtube.com/watch?v=TVbiRywszco
- https://www.youtube.com/watch?v=-S2XckLOiO8
- https://www.youtube.com/watch?v=QYNJC9EhxIc
- https://www.youtube.com/watch?v=4QBEC2ku6ws
- https://www.youtube.com/watch?v=DSvBXXnZv34&list=PLW6YlvHa65xg5asFyEm6hx0wjHNcaVpTT

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Role Play
- Flipped classroom
- Assessment Methods Marks (opt two Learning Activities)
    - Quiz
    - Programming Assignment
    - Gate Based Aptitude Test
    - MOOC Assignment for selected Module

Virtual Labs:

- **https://cse29-iiith.vlabs.ac.in/**

Analog Communication Laboratory			
Course Code	24ECL45	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	0:0:2	**SEE Marks**	50
Credits	01	**Total Marks**	100
Contact Hours	12 Labslots	**Exam Hours**	3
Examination type (SEE)	Practical		

Prerequisites:

- Understanding of signal types, Fourier series, Fourier transforms, modulation, and system response.
- Familiarity with modulation techniques such as AM, FM, PM, DSB-SC, and SSB.
- Basics of amplifiers, oscillators, and filters used in modulation and demodulation circuits.

Course Objectives:

This laboratory course enables students to

- Understand the basic concepts of AM and FM modulation and demodulation.
- Design and analyse the electronic circuits used for AM and FM modulation and demodulation circuits.
- Understand the sampling theory and design circuits which enable sampling and reconstruction of analog signals.
- Design electronic circuits to perform pulse amplitude modulation, pulse position modulation and pulse width modulation.

	Experiments
1	Design a collector Modulator circuit and demodulate the signal using diode detector.
2	Design a balanced modulator circuit using diodes
3	Design a Frequency modulator using IC 8038
4	Design and plot the frequency response of pre-emphasis and De-emphasis Circuits
5	Design and test Pulse amplitude modulation and demodulation.
6	Generation and Detection of Pulse position Modulation
7	Generation and Detection of Pulse Width Modulation
8	PLL Frequency Synthesizer

9	Data formatting and Line Code Generation
10	PCM Multiplexer and Demultiplexer
11	Frequency Modulation and Demodulation using MATLAB.
12	Generation and detection of Pulse Code Modulation using MATLAB

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. Illustrate the AM generation and detection using suitable electronic circuits.(PO-1,PO-8,PSO-1, PSO-2)
2. Design of FM circuits for modulation, demodulation and noise suppression. .(PO-1,PO-3.PO-8,PSO-1, PSO-2)
3. Design and test the sampling, Multiplexing and pulse modulation techniques using electronic hardware. .(PO-1,PO-3,PO-8,PSO-1, PSO-2)
4. Design and Demonstrate the electronic circuits used for RF transmitters and receivers.(PO-1PO-3,,PO-8,PSO-1, PSO-2)

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are 50 Marks.

The split-up of CIE marks for record/ journal and test are in the ratio 60:40.

•Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.

•Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.

•Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).

•Weightage to be given for neatness and submission of record/write-up on time.

•Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.

•In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.

•The suitable rubrics can be designed to evaluate each student's performance and learning ability.

•The marks scored shall be scaled down to 20 marks (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

•SEE marks for the practical course are 50 Marks.

•All laboratory experiments are to be included for practical examination.

•(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.

•Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.

•Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

•Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1.Louis E Frenzel, Principles of Electronic Communication Systems, 3rd Edition, Mc Graw Hill Education (India) Private Limited, 2016. ISBN: 978-0-07-066755-6.

Virtual Lab Links:

- https://ecelabs.nitk.ac.in/Analog-Communication-Lab

Operating systems		Semester	4
Course Code	**24EC46A**	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	2:2:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

- To demonstrate the need and different types of OS
- To discuss suitable techniques for management of different resources
- To analyse different memory, storage, and file system management strategies.

Teaching-Learning Process (General Instructions)

These are sample strategies; which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) does not mean only the traditional lecture method, but different types of teaching methods may be adopted to achieve the outcomes.
2. Utilize video/animation films to illustrate the functioning of various concepts.
3. Promote collaborative learning (Group Learning) in the class.
4. Pose at least three HOT (Higher Order Thinking) questions in the class to stimulate critical thinking.
5. Incorporate Problem-Based Learning (PBL) to foster students' analytical skills and develop their ability to evaluate, generalize, and analyze information rather than merely recalling it.
6. Introduce topics through multiple representations.
7. Demonstrate various ways to solve the same problem and encourage students to devise their own creative solutions.
8. Discuss the real-world applications of every concept to enhance students' comprehension.
9. Use any of these methods: Chalk and board, Active Learning, Case Studies

Module – 1

Introduction: What operating systems do; Computer System organization; Computer System Organization, Computer System architecture; Operating System operations; Resource Management

Operating System Structures: Operating System Services, User and Operating System interface; System calls, Application Program Interface, Types of system calls;

Textbook 1: Chapter 1: 1.1, 1.2, 1.3,1.4, 1.5 Chapter 2: 2.1, 2.2 (2.2.1, 2.2.2), 2.3 (2.3.2, 2.3.3)

Module – 2

Process Management: Process concept; Process scheduling; Operations on processes; Interprocess Communication

Multi-threaded Programming: Overview; Multithreading models, Thread Libraries

Textbook 1: Chapter 3: 3.1-3.4, Chapter 4: 4.1, 4.3 5, 4.4

Module – 3 (10 Hours)

CPU Scheduling: Basic Concepts, Scheduling criteria, Scheduling algorithms, Thread Scheduling,

Process Synchronization: Synchronization: The critical section problem; Peterson's solution; Semaphores; Classical problems of synchronization;

Textbook 1: Chapter 5: 5.1, 5.2,5.3.1, 5.3.2, 5.3.3, 5.3.4, 5.4 Chapter 6: 6.1, 6.2.,6.3, 6.6

Module – 4 (11 Hours)

Deadlocks: System model; Deadlock characterization; Methods for handling deadlocks; Deadlock prevention; Deadlock avoidance; Deadlock detection and recovery from deadlock. Memory Management: Background; Contiguous memory allocation; Paging; Structure of page table

Textbook 1: Chapter 8: 8.1-8.8 Textbook 1: Chapter 9: 9.1-9.4 (9.4.1, 9.4.2)

Module – 5 (10 Hours)

Virtual Memory Management: Background; Demand paging; Copy-on-write; Page replacement;

File System Interface: File concept; Access methods; Directory Structure, Protection, File System Implementation: File System Structure, File System Operations,

File System Internals: File Systems, File System Mounting; Partition and Mounting, File sharing;

Textbook 1: Chapter 10: 10.1-10.3, 10.4 (10.4.1, 10.4.2, 10.4.4.) Chapter 13: 13.1, 13.2, 13.3 (13.3.1, 13.3.2, 13.3.3), 13.4 (13.4.1, 13.4.2) Chapter 15: 15.1-15.4

Course outcomes (Course Skill Set)

At the end of the course, the student will be able to:

1. Explain the fundamentals of operating systems.
2. Apply appropriate CPU scheduling algorithm for the given scenarios.
3. Analyse the various techniques for process synchronization and deadlock handling.
4. Apply the various techniques for memory management
5. Analyse the importance of File System Mounting and File Sharing

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

● For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.

● The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered

● Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.

● For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.

2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.

3. The students have to answer 5 full questions, selecting one full question from each module.

4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books:

1. Abraham Silberschatz, Peter Baer Galvin, Greg Gagne, Operating System Principles 10th edition, Wiley-India, 2015

Reference Books

2. Ann McHoes Ida M Fylnn, Understanding Operating System, Cengage Learning, 6th Edition, 2010

3. D.M Dhamdhere, Operating Systems: A Concept Based Approach 3rd Ed, McGraw-Hill, 2013, P.C.P. Bhatt, An Introduction to Operating Systems: Concepts and Practice 4th Edition, PHI(EEE), 2014.

4. William Stallings Operating Systems: Internals and Design Principles, 6th Edition, Pearson, 2008

Reference Books:

1. Akshay Kulkarni, Adarsha Shivananda, "Natural Language Processing Recipes - Unlocking Text Data with Machine Learning and Deep Learning using Python", Apress, 2019.

2. T V Geetha, "Understanding Natural Language Processing – Machine Learning and Deep Learning Perspectives", Pearson, 2024.

3. Gerald J. Kowalski and Mark.T. Maybury, "Information Storage and Retrieval systems", Kluwer Academic Publishers.

YouTube Video Links:

1.https://archive.nptel.ac.in/courses/106/105/106105214/
2.https://archive.nptel.ac.in/courses/106/102/106102132/

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Students are expected to prepare animated PPT to illustrate the different types of Process Scheduling and Paging. (10 Marks)
- Students are required to prepare detailed case study report on Deadlocks OR Students can illustrate deadlock using any programming language (15 Marks)

Industrial Internet of Things			
Course Code	24EC46B	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	3:0:0	**SEE Marks**	50
Credits	03	**Total Marks**	100
Contact Hours	40	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Basic Knowledge of IoT Concepts
- Computer Networks and Communication Protocols
- Embedded Systems Fundamentals
- Basics of Industrial Automation

Course Objectives:

- Introduce how IoT has become a game changer in the new economy where the customers are looking for integrated value
- Bring the IoT perspective in thinking and building solutions
- Introduce the tools and techniques that enable IoT solution and Security aspects

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Demonstration based Teaching

Module-1	**8 Hours**

Introduction: Introduction to IOT, What is IIOT? IOT Vs. IIOT, History of IIOT, Components of IIOT - Sensors, Interface, Networks, People &Process, Hype cycle, IOT Market, Trends& future Real life examples, Key terms – IOT Platform, Interfaces, API, clouds, Data Management Analytics, Mining &Manipulation; Role of IIOT in Manufacturing Processes Use of IIOT in plant maintenance practices, Sustainability through Business excellence tools Challenges & Benefits in implementing IIOT

Module-2	**8 Hours**

Architecture: Overview of IOT components ;Various Architectures of IOT and IIOT, Advantages & disadvantages,

Industrial Internet - Reference Architecture; IIOT System components: Sensors, Gateways, Routers, Modem, Cloud brokers, servers and its integration, WSN, WSN network design for IOT

Module-3	**8 Hours**

Sensor and Interfacing: Introduction to sensors, Transducers, Classification, Roles of sensors in IIOT , Various types of sensors , Design of sensors, sensor architecture, special requirements for IIOT sensors, Role of actuators, types of actuators. Hardwire the sensors with different protocols such as HART, MODBUS-Serial & Parallel, Ethernet, BACNet , Current, M2M etc

Module-4 **8 Hours**

Protocols and Cloud: Need of protocols; Types of Protocols, Wi-Fi, Wi-Fi direct, Zigbee, Z wave, Bacnet, BLE, Modbus, SPI , I2C, IIOT protocols –COAP, MQTT,6lowpan, lwm2m, AMPQ IIOT cloud platforms : Overview of cots cloud platforms, predix, thingworks, azure etc. Data analytics, cloud services, Business models: Saas, Paas, Iaas.

Module-5 **8 Hours**

Privacy, Security and Governance: Introduction to web security, Conventional web technology and relationship with IIOT, Vulnerabilities of IoT, Privacy, Security requirements, Threat analysis, Trust, IoT security tomography and layered attacker model, Identity establishment, Access control, Message integrity, Non-repudiation and availability, Security model for IoT, Network security techniques Management aspects of cyber security

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Describe IOT,IIOT

CO2 :Understand, design and develop the real life IoT applications using off the shelf hardware and software

CO3 :Understand various IoT Layers and their relative importance

CO4 :Study various IoT platforms and Security

CO5 :Realize the importance of Data Analytics in IoT

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the regulations; if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Textbook:

1. Daniel Minoli, "Building the Internet of Things with IPv6 and MIPv6: The Evolving World of M2M Communications", ISBN: 978-1-118-47347-4, Willy Publications
2. Bernd Scholz-Reiter, Florian 2. Michahelles, "Architecting the Internet of Things", ISBN 978-3- 642-19156-5 e- ISBN 978-3-642-19157-2, Springer

Reference Books:

1. Hakima Chaouchi, " The Internet of Things Connecting Objects to the Web" ISBN : 978-1- 84821-140-7, Willy Publications
2. Olivier Hersent, David Boswarthick, Omar Elloumi, The Internet of Things: Key Applications and Protocols, ISBN: 978-1-119-99435-0, 2 nd Edition, Willy Publications
3. Inside the Internet of Things (IoT), Deloitte University Press
4. Internet of Things- From Research and Innovation to Market Deployment; By Ovidiu & Peter; River Publishers Series
5. Five thoughts from the Father of the Internet of Things; by By Phil Wainewright - Kevin Ashton
6. How Protocol Conversion Addresses IIoT Challenges: White Paper By RedLion.

Web links and Video Lectures(e-Resources):

- **https://youtube.com/playlist?list=PLdYcKdE5uRf1lvXANoaOaYQTe4DrINPZO&si=rc1s_Jupr9yS6yFJ**
- **https://youtube.com/playlist?list=PLbRMhDVUMngdcLdH4-YF1uJI4IuhcDZPR&si=-xr_q3kFXZxw6pHC**
- **https://youtu.be/5042oX28Tb8?si=7g7IFfFKF_3ycryJ**

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Role Play
- Flipped classroom
- Assessment Methods for 25 Marks
    - Case Study
    - Mini Project

MICROCONTROLLERS			
Course Code	24EC46C	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	3:0:0	**SEE Marks**	50
Credits	03	**Total Marks**	100
Contact Hours	40	**Exam Hours**	3
Examination type (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Digital Logic Design
- Basic Programming Skills
- Computer Architecture Basics
- Understanding of Algorithms
- Basic Mathematics
- Problem-Solving Skills

Course Objectives:

- To understand the difference between Microprocessor and Microcontroller and embedded microcontrollers.
- To analyze the basic architecture of 8051microcontroller.
- To Program 8051 microcontroller using Assembly Language and C.
- To understand the operation and use of inbuilt Timers/Counters and Serial port of 8051
- To understand the interrupt structure of 8051 and Interfacing I/O devices using I/O ports of 8051.

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. ICT based Teaching
3. Problem based learning
4. Demonstration based Teaching

Module-1	**8 Hours**

Microcontroller: Microprocessor Vs Microcontroller, Micro controller & Embedded Processors, Overview of 8051 family, Processor Architectures- Harvard Vs Princeton & RISC Vs CISC , 8051 Architecture- Registers, Pin diagram, I/O ports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing, Programming the 8051

Text book 1-Chapter-1:1.1,**Text book 2**- Chapter-1:1.0,1.1,1.2,Chapter-3:3.0,3.1,3.2,3.3,
Text book 3-Chapter -5:Pg 5-9

Module-2	**8 Hours**

Instruction Set: Introduction to 8051 Assembly programming, Structure of Assembly Language, Assembling & running an 8051 Program,8051 Addressing Modes, Data Transfer Instructions, Arithmetic instructions, Logical Instructions, Jump & Call Instructions Stack & Subroutine Instructions of 8051 (with examples in assembly Language).

Text book 1- Chapter-2:2.2,2.3,**Text book 2**- Chapter 5,6,7,8

Module-3	**8 Hours**

Timers/Counters & Serial port programming: Basics of Timers & Counters, Data types & Time delay in the 8051 using C, Programming 8051 Timers, Mode 1 & Mode 2 Programming, Counter Programming (Assembly Language only)

Basics of Serial Communication, 8051 Connection to RS232, Programming the 8051 to transfer data serially & to receive data serially using C.

Text book 2- Chapter-3:3.4, **Text book 1-** Chapter-7:7.1,Chapter-9: 9.1,9.2**, Text book 2**- 3.5, **Text book 1**- Chapter -10:10.1,10.2,10.3(except assembly language programs),10.5

Module-4	**8 Hours**

Interrupt Programming: Basics of Interrupts, 8051 Interrupts, Programming Timer Interrupts, Programming Serial Communication Interrupts, Interrupt Priority in 8051 (Assembly Language only)

Text book 2:Chapter-3: 3.6, **Text book 1**:Chapter-11:11.1,11.2,11.4,11.5

Module-5	**8 Hours**

I/O Port Interfacing & Programming: I/O Programming in 8051 C, LCD interfacing, Keyboard interfacing, DAC 0808 Interfacing, ADC 0804 interfacing, Stepper motor interfacing, DC motor control & Pulse Width Modulation (PWM) using C only.

Text book 1-Chapter-7:7.2,Chapter-12:12.1,12.2,Chapter-13:13.1,13.2, Chapter17:17.2,17.3 Case Studies: Traffic Light Controller using Timers & Delays

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

CO1: Describe the difference between Microprocessor and Microcontroller, Types of Processor Architectures and Architecture of 8051Microcontroller. (PO – 1,2,3, PSO – 1,3)

CO2: Discuss the types of 8051 Microcontroller Addressing modes & Instructions with Assembly Language Programs. (PO – 1,2,3, PSO – 1,3)

CO3: Explain the programming operation of Timers/Counters and Serial port of 8051 Microcontroller. (PO – 1,2,3, PSO – 1,3)

CO4: Illustrate the Interrupt Structure of 8051 Microcontroller & its programming. (PO – 1,2,3, PSO – 1,3)

CO5: Develop C programs to interface I/O devices with 8051 Microcontroller. (PO – 1,2,3, PSO – 1,3)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the regulations shall be considered; if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Textbook:

1. The "8051 Microcontroller and Embedded Systems – Using Assembly and C", Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollind. Mckinlay; Phi, 2006 / Pearson, 2006.

2. "The 8051 Microcontroller", Kenneth j. Ayala, 3rd edition, Thomson/Cengage Learning.
3. "Programming And Customizing The 8051 Microcontroller".,Myke Predko Tata Mc Graw-Hill Edition 1999 (reprint 2003).

Reference Books:

1. The 8051 Microcontroller Based Embedded Systems", Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4.
2. "Microcontrollers: Architecture, Programming, Interfacing and System Design", Raj Kamal, Pearson Education, 2005.

Web links and Video Lectures(e-Resources):

- https://elearning.vtu.ac.in/esk/P3/econtent/18EC46/index.php
- https://www.youtube.com/watch?v=pA6K5NgWTow
- https://www.youtube.com/playlist?list=PLaKtTm3mCI2alKlTvvJE4KqSEFjU6phDn
- **https://digimat.in/nptel/courses/video/108105102/L23.html**
- https://www.mindluster.com/certificate/959/8051-Microcontroller-programming-video
- **https://technobyte.org/8051-microcontroller-course**
- **https://www.classcentral.com/course/udemy-the-8051-microcontroller-35560**

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Flipped classroom
- Assessment Methods for 25 Marks (opt two Learning Activities)
  - Case Studies
  - Programming Assignment
  - Gate Based Aptitude Test
  - Certification course

Data Structures Using C			
Course Code	24EC46D	CIE Marks	50
Teaching Hours/Week (L: T:P)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	Theory		

Prerequisites:

The students should have knowledge on

- Basic Knowledge of C Programming
- Functions and Recursion
- Pointers and Dynamic Memory Allocation
- Arrays and Strings

COURSE OBJECTIVES:

The objectives of this course are to:

1. Develop proficiency in designing and implementing fundamental data structures.
2. Learn various sorting and searching algorithms and analyze their time complexity.
3. Understand algorithmic problem-solving techniques, including recursion.
4. Explore advanced data structures like trees, graphs, and hash tables.
5. Apply data structures and algorithms knowledge to solve real-world programming challenges efficiently.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. The lecturer's approach (L) does not have to be limited to traditional methods of teaching. It is possible to incorporate alternative and effective teaching methods to achieve the desired outcomes.
2. Utilize videos and animations to illustrate the functioning of different techniques used in the manufacturing of smart materials.
3. Foster collaborative learning exercises within the classroom to encourage group participation and engagement.
4. Pose a minimum of three Higher Order Thinking (HOT) questions during class discussions to stimulate critical thinking among students.
5. Implement Problem-Based Learning (PBL) as an approach that enhances students' analytical skills and nurtures their ability to design, evaluate, generalize, and analyze information, rather than solely relying on rote memorization.

Module-1

Arrays:1D,2D and multidimensional.

Pointers: Definition and Concepts, Array of pointers, Structures and unions. Array of structures, pointer arrays, pointer to structures. Passing pointer variable as parameter in functions, Dynamic memory allocation: malloc(), calloc(), realloc() and free function. Introduction to data structures and algorithms

Text book 1 -Chapter-1.1-1.3 except Rational Numbers.

Text Book 2, chapter-2

Module-2
The Stack – Definition and examples, primitive operations, Example. Representing Stacks in C, Example:Infix,Postfix and Prefix,converting an Expression from Infix to Prefix and Program. Text Book -1-Chapter – 2.1-2.3 Recursion – Recursive Definition and Processes, Recursion in C, Writing Recursive Programs. Recursions - Text Book -1-Chapter – 3.1-3.3
Module-3
Queues and Lists – The Queue and its sequential representation, Linked Lists, Lists in C. Other Lists structures – Circular Lists, Stacks, Queues as circular list. The Josephus problem ,doubly linked lists. Linked lists and Queues - Text Book -1-Chapter – 4.1-4.3,4.5
Module-4
Trees – Binary Trees, binary tree representations, Huffman algorithm, Trees and their applications. Searching – Basic searching Techniques, Tree Searching. Trees - Text Book -1-Chapter – 5.1-5.3,5.5,7.1,7.2
Module-5
Hashing – Introduction, Static Hashing, Dynamic Hashing Text Book 3 -8.1 – 8.3 Graphs - Graph representation, Elementary graph operations, Minimum cost spanning Trees – Kruskal's Algorithm, Prim's algorithm Text Book 3 - 6.1,6.2,6.3.1,6.3.2
Course Outcomes (COs) (Course Skill Set) At the end of the course, the student will be able to: CO1; Master the implementation and application of key data structures in programming. (PO-1,2,5) CO2: Demonstrate the ability to analyze algorithm efficiency and optimize code. (PO-1,2,5) CO3: Solve complex problems by applying algorithmic strategies and techniques. (PO-1,2,5) CO4: Design and implement algorithms for tasks involving searching, sorting, and graph traversal. (PO-1,2,5) CO5: Utilize data structures and algorithms to enhance software performance and scalability. (PO-1,2,5)

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination (SEE):

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

Suggested Learning Resources:

TEXT BOOKS:

1. Data Structures using C and C++, Yedidyah, Augenstein, Tannenbaum, 2nd Edition, Pearson Education, 2007.
2. Data Structures using C, Reema Thareja, 2nd Edition, Oxford University Press, 2011
3. Fundamentals of Data structures in C, 2nd Edition, Horowitz, Sahni, Anderson freed Universities Press,2008

REFERENCEBOOKS:

1. Reema Thareja, Computer fundamentals and programming in C, second edition, Oxford University Press.
2. Gilberg and Forouzan, Data Structures: A Pseudo-code approach with C, 2ndEd, CengageLearning,2014.

Web links and Video Lectures (e-Resources):

- https://archive.nptel.ac.in/courses/106/102/106102064/
- https://archive.nptel.ac.in/courses/106/106/106106127/
- https://nptel.ac.in/courses/106102064
- http://elearning.vtu.ac.in/econtent/courses/video/CSE/06CS35.html
- https://nptel.ac.in/courses/106/105/106105171/
- http://www.nptelvideos.in/2012/11/data-structures-and-algorithms.html
- http://elearning.vtu.ac.in/econtent/courses/video/CSE/06CS43.html
- https://nptel.ac.in/courses/106/101/106101060/

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Real world problem solving using group discussion.

- Back/Forward stacks on browsers.
- Undo/Redo stacks in Excel or Word.
- Linked list representation of real-world queues -Music player, image viewer
- Real world problem solving and puzzles using group discussion. E.g., Fake coin identification, Peasant, wolf, goat, cabbage puzzle, Konigsberg bridge puzzle etc.,
- Demonstration of solution to a problem through programming.

Octave / Scilab for Signals			
Course Code	24EC47A	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	0:0:2	**SEE Marks**	50
Credits	01	**Total Marks**	100
Contact Hours	12	**Exam Hours**	2
Examination type (SEE)	Practical		

Prerequisites:

The students should have knowledge on

- Basic Signals and Systems
- Problem Solving Skills

Course Objectives:

- **Preparation**: To prepare students with fundamental knowledge/ overview in the field of signals and processing.
- **Core Competence**: To equip students with a basic foundation in electronic engineering and mathematics fundamentals required for comprehending the operation and application of signal processing.
- **Professionalism & Learning Environment**: To inculcate in students an ethical and professional attitude by providing an academic environment inclusive of effective communication, teamwork, ability to relate engineering issues to a broader social context, and life-long learning needed for a successful professional career.

Teaching-Learning Process (General Instructions)

Teachers can use following strategies to accelerate the attainment of the various course outcomes.

1. Chalk and Talk with Black Board
2. Hands on

Sl.No	Experiments
1	Create a Matrix and perform the following Operations (Transpose, Inverse, Multiplication)
2	Solving a System of Linear Equations
3	Generate a Sine Wave (Continuous Signal), add Noise to a Signal and plot both
4	Convert time domain signal to frequency domain and plot its magnitude
5	Remove high frequency noise from a signal using filter

6	Generation and visualization of standard test signals (both continuous and discrete time).
7	**Signal Manipulations** Signal addition, subtraction, and multiplication Even and odd decomposition of signals
8	Perform the amplitude scaling, time shifting, time scaling operations on step signal.
9	Verify the Sampling theorem.
10	generating and plotting Impulse and step response of basic discrete systems.
11	Determine the linear convolution of two given point sequences. Verify the result using theoretical computations.
12	Determine Circular convolution of two given point sequences. Verify the result using theoretical computations.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Create matrix and solve leaner equations (PO – 1,2,3,5 PSO – 1,3)
- Design and verify the computation of discrete signals using. (PO – 1,2,3,5 PSO – 1,3)
- Demonstrate and verify the sampling theorem. (PO – 1,2,3,5 PSO – 1,3)
- Design, demonstrate and visualize different real-world signals. (PO – 1,2,3,5 PSO – 1,3)
- Determine the response of the system. (PO – 1,2,3,5 PSO – 1,3)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.Theminimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination)taken together. Continuous Internal Evaluation(CIE): CIE marks for the practical course are 50 Marks. The split-up of CIE marks for record/journal and test are in the ratio 60:40.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment writeup will be evaluated for 10marks.
- Total marks scored by the students are scaled down to 30 marks(60%ofmaximummarks).
- Weightage to be given for neatness and submission of record/write-upon time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.

- In a test, writeup, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to 20 marks(40% of the maximum marks). The Sum of scaled-down marks scored in the report write-up/journal and marks of a Test is the total CIE marks scored by the student.

Semester End Evaluation(SEE):

- SEE marks for the practical course are 50Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question(experiment)fromthequestionslotpreparedbytheexaminersjointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in - 60%,Viva- voce 20% of maximum marks. SEE for practicalshall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks(however, based on course type, rubrics shall be decided by the examiners) Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero. The minimum duration of SEE is 03 hours

Suggested Learning Resources:

1. Digital Signal Processing Using MATLAB, John G Proakis and Vinay K Ingle, Cengage Learning, 2011

Web links and Video Lectures(e-Resources):

- **https://www.youtube.com/watch?v=rCxsR1C85NI**
- **https://www.youtube.com/watch?v=sYg_-ebfzrY**
- **https://www.youtube.com/watch?v=mDzH7zodKww**
- **https://www.youtube.com/watch?v=kBu1rBXnSps**
- **https://www.youtube.com/watch?v=8Sx_ruSfJ0s&t=68s**

MICROCONTROLLERS LAB			
Course Code	24EC47B	CIE Marks	50
Teaching Hours/Week(L:T:P)	0:0:2	SEE Marks	50
Credits	01	Total Marks	100
		Exam Hours	3
Examination type(SEE)	Practical		

Prerequisites:

The students should have knowledge on

- Digital Logic Design
- Basic Programming Skills
- Understanding of Algorithms
- Basic Mathematics
- Problem-Solving Skills

Course objectives:

- To understand the basic programming of Microcontrollers.
- To develop the 8051 Microcontroller-based programs for various applications using Assembly Language & C Programming.
- To program 8051 Microcontroller to control an external hardware using suitable I/O ports.

Note	Execute the following experiments by using Keil Microvision Simulator (any 8051 Microcontroller can be chosen as the target) and Hardware Interfacing Programs using 8051 Trainer Kit.
Sl.No	**I. Assembly Language Programming**
Data Transfer Programs:	
1	Write an ALP to move a block of n bytes of data from source (20h) to destination (40h) using Internal-RAM.
2	Write an ALP to move a block of n bytes of data from source (2000h) to destination (2050h) using External RAM.
3	Write an ALP To exchange the source block starting with address 20h, (Internal RAM) containing N (05) bytes of data with destination block starting with address 40h (Internal RAM).
4	Write an ALP to exchange the source block starting with address 10h (Internal memory), containing n (06) bytes of data with destination block starting at location 00h (External memory).
Arithmetic & Logical Operation Programs:	
5	Write an ALP to perform addition, subtraction, multiplication and division of the byte in RAM at 34h and 35h, store the result in the register R5 (LSB) and R6 (MSB), using Indirect Addressing Mode.
6	Write an ALP to arrange the numbers in Ascending & Descending order.
7	Write an ALP to find Largest & Smallest number from a given array starting from 20h & store it in Internal Memory location 40h.
Counter Operation Programs:	
8	Write an ALP for Decimal UP and DOWN Counter.
9	Write an ALP for Hexadecimal UP and DOWN Counter.
II.Hardware Interfacing Programs	
10	Write an 8051 C Program to rotate stepper motor in Clock & Anti-Clockwise direction.
11	Write an 8051 C program to Generate Sine & Square waveforms using DAC interface.
12	Write an 8051 C program to interface LCD

Course outcomes(Course Skill Set):

At the end of the course the student will be able to:

CO1: Write a Assembly Language/C programs in 8051 for solving simple problems that manipulate input data using different instructions. (PO – 1,2,3, PSO – 1,3)

CO2: Develop Testing and experimental procedures on 8051 Microcontroller, Analyze their operation under different cases. (PO – 1,2,3, PSO – 1,3)

CO3: Develop programs for 8051 Microcontroller to implement real world problems. (PO – 1,2,3, PSO – 1,3)

CO4: Develop Microcontroller applications using external hardware interface. (PO – 1,2,3, PSO – 1,3)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.Theminimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination)taken together.

Continuous Internal Evaluation(CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write- up will be evaluated for 10marks.
- Total marks scored by the students are scaled down to **30 marks**(60%ofmaximummarks).
- Weightage to be given for neatness and submission of record/write-upon time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, writeup, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks**(40% of the maximum marks). The Sum of scaled-down marks scored in the report write-up/journal and marks of a Test is the total CIE marks scored by the student.

Semester End Evaluation(SEE):

- SEE marks for the practical course are 50Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question(experiment)fromthequestionslotpreparedbytheexaminersjointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in - 60%,Viva- voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks(however, based on course type,
rubrics shall be decided by the examiners) Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero. The minimum duration of SEE is 03 hours

Suggested Learning Resources:

1. "The 8051 Microcontroller: Hardware, Software and Applications" ,V Udaya shankara and M S Mallikarjuna Swamy, McGraw Hill Education, 1st edition,2017.

Web links and Video Lectures(e-Resources):

- **https://vlab.co.in/broad-area-electronics-and-communication**
- **https://edsim51.com**
- **https://www.labcenter.com**
- **https://emu8086.com/emulator.html**

Virtual Lab Links:

- **https://vlab.co.in**

Basics of IoT and its Applications Lab			
Course Code	**24EC47C**	CIE Marks	50
Teaching Hours/Week (L:T:P)	0:0:2	SEE Marks	50
Credits	01	Exam Hours	3
Examination type (SEE)	**Practical**		

Prerequisites:

The students should have knowledge on

- Digital Logic Design
- Basic Programming Skills
- Computer Architecture Basics

Course Objectives:

This course will enable students to

- To impart necessary and practical knowledge of components of the Internet of Things
- To develop skills required to build real-life IoT-based projects.

Sl.No.	Experiments
1(i)	To interface LED/Buzzer with Arduino /Raspberry Pi and write a program to 'turn ON' LED for 1 sec after every 2 seconds.
1(ii)	To interface the Push button/Digital sensor (IR/LDR) with Arduino /Raspberry Pi and write a program to 'turn ON' LED when a push button is pressed or at sensor detection.
2 (i)	To interface the DHT11 sensor with Arduino /Raspberry Pi and write a program to print temperature and humidity readings.
2(ii)	To interface OLED with Arduino /Raspberry Pi and write a program to print its temperature and humidity readings.
3	To interface the motor using a relay with Arduino /Raspberry Pi and write a program to 'turn ON' the motor when a push button is pressed.
4(i)	Write an Arduino/Raspberry Pi program to interface the Soil Moisture Sensor.
4(ii)	Write an Arduino/Raspberry Pi program to interface the LDR/Photo Sensor.
5	Write a program to interface an Ultrasonic Sensor with Arduino /Raspberry Pi.
6	To interface Bluetooth with Arduino/Raspberry Pi and write a program to send sensor data to smart phone using Bluetooth.
7	To interface Bluetooth with Arduino/Raspberry Pi and write a program to turn LED ON/OFF when 1/0 is received from smart phone using Bluetooth
8	Write a program on Arduino/Raspberry Pi to upload temperature and humidity data to thingspeak cloud.
9	Write a program on Arduino/Raspberry Pi to retrieve temperature and humidity data from thingspeak cloud.
10	Write a program to interface LED using Telegram App.
11	Write a program on Arduino/Raspberry Pi to publish temperature data to the MQTT broker

12	Write a program on Arduino / Raspberry Pi to subscribe to the MQTT broker for temperature data and print it.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Explain the Internet of Things and its hardware and software components.
2. Interface I/O devices, sensors & communication modules.
3. Remotely monitor data and control devices.
4. Develop real-life IoT-based projects.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment will be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session. The record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
-
- The total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage is to be given for neatness and submission of record/write-up on time.
- The department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted within the schedule mentioned in the university's academic calendar.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.The minimum duration of SEE is 02 hours.

Suggested Learning Resources:

- Vijay Madisetti, Arshdeep Bahga, Internet of Things. "A Hands-on Approach", University Press
- Dr. SRN Reddy, Rachit Thukral, and Manasi Mishra, "Introduction to Internet of Things: A Practical Approach", ETI Labs
- Pethuru Raj and Anupama C Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", CRC Press
- Jeeva Jose, "Internet of Things", Khanna Publishing House, Delhi
- Adrian McEwen, "Designing the Internet of Things", Wiley
- Raj Kamal, "Internet of Things: Architecture and Design", McGraw Hill

Web links and Video Lectures(e-Resources):

- https://elearning.vtu.ac.in/esk/P3/econtent/18EC46/index.php
- https://www.youtube.com/watch?v=pA6K5NgWTow
- https://www.youtube.com/playlist?list=PLaKtTm3mCI2alKlTvvJE4KqSEFjU6phDn
- **https://digimat.in/nptel/courses/video/108105102/L23.html**
- https://www.mindluster.com/certificate/959/8051-Microcontroller-programming-video
- **https://technobyte.org/8051-microcontroller-course**
- **https://www.classcentral.com/course/udemy-the-8051-microcontroller-35560**

Activity Based Learning (Suggested Activities in Class)/Practical Based Learning

- Flipped classroom
- Assessment Methods for 25 Marks (opt two Learning Activities)
    - Case Studies
    - Programming Assignment
    - Gate Based Aptitude Test
    - Certification course

System Verilog		Semester	4
Course Code	**24EC47D**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	3
Examination type (SEE)	**Practical**		

Pre-Requisites: Digital fundamentals, Verilog

Course Objectives:

This course will enable students to

- To understand the importance of design verification in VLSI
- To apply object-oriented programming (OOP) concepts in System Verilog for verification.
- To recognize various verification tools.
- To analyze different levels of verification
- To develop and Analyze Test bench Components
- To integrate test bench components into a structured verification environment.

Simulation experiments using software tools like Modelsim, cadence-xcelium, EDA playground

Sl.No.	Experiments
1	Usage of System Verilog data types using examples(Arrays, Queues and Enumerated)
2	Usage of System Verilog data types using examples(class type, inheritance and polymorphism)
3	Usage of system Verilog randomization with constraints using examples (Inline, solve before etc.,)
4	Simulation of checkers and assertions
5	Design and verification of full adder self-checking test bench
6	Design and functional coverage analysis for single and dual port RAM
7	Design and code coverage analysis for synchronous and Asynchronous FIFO
8	Design and verification of APB protocol using layered test bench
9	Design and verification FIFO using layered test bench
10	Design and verification of USB protocol using layered test bench

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Appreciate the significance of design verification in VLSI design process
2. Apply System Verilog constructs for verifying the design.
3. Design and analyze test bench components
4. Create verification environment using System Verilog

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment will be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session. The record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- The total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage is to be given for neatness and submission of record/write-up on time.
- The department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted within the schedule mentioned in the university's academic calendar.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners) Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

- The minimum duration of SEE is 02 hours

Suggested Learning Resources/Weblinks/ Digital library/Virtual labs/E Text books:

- https://opencourses.gr/index.xhtml?ln=en
- https://github.com/topics/systemverilog-project
- https://edaplatground.com/
- System Verilog for Verification by Chris Spear
- System Verilog Assertions and Functional Coverage by Ashok Mehta
- Writing test benches using system Verilog by Janick Bergeron

Universal Human Values			
Course Code	24UH48	**CIE Marks**	50
Teaching Hours/Week (L: T: P)	2:0:0	**SEE Marks**	50
Credits	02	**Total Marks**	100
Contact Hours	25	**Exam Hours**	03
Examination type (SEE)	Theory		

Prerequisites: NIL

Course Objectives:

This course is intended to:

- To help the students appreciate the essential complementarity between 'VALUES' and 'SKILLS' to ensure sustained happiness and prosperity which are the core aspirations of all human beings.
- To facilitate the development of a Holistic perspective among students towards life and profession as well as towards happiness and prosperity based on a correct understanding of the Human reality and the rest of existence. Such a holistic perspective forms the basis of Universal Human Values and movement towards value-based living in a natural way.
- To highlight plausible implications of such a Holistic understanding in terms of ethical human conduct, trustful and mutually fulfilling human behaviour and mutually enriching interaction with Nature.
- This course is intended to provide a much-needed orientation input in value education to the young enquiring minds.

Teaching-Learning Process (General Instructions):

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. The methodology of this course is explorational and thus universally adaptable. It involves a systematic and rational study of the human being vis-à-vis the rest of existence.
2. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the activities will develop students' theoretical and applied skills.
3. State the need for UHV activities and its present relevance in the society and provide real-life examples.
4. Support and guide the students for self-study activities.
5. You will also be responsible for assigning homework, grading assignments and quizzes, and documenting students' progress in real activities in the field.
6. This process of self-exploration takes the form of a dialogue between the teacher and the students to begin with, and then to continue within the student in every activity, leading to continuous self-evolution.
7. Encourage the students for group work to improve their creative and analytical skills.

Module- 1 **5 Hours**

Introduction to Value Education: Understanding the need, Basic Guidelines, Content and process for Value Education; Self-Exploration: What is it? - its content and process, Natural Acceptance and Experiential Validation- as the mechanism for self-exploration; Continuous Happiness and Prosperity: A look at basic Human Aspirations; Right understanding, Relationship and Physical Facilities- the basic requirements for fulfillment of aspirations of every human being with their correct priority; Understanding Happiness and Prosperity correctly- A critical appraisal of the current scenario; Method to fulfill the above human aspirations: understanding and living in harmony at various levels.

Module- 2 **5 Hours**

Understanding Harmony in the Human Being: Understanding Human being as the Co-existence of the Self and the Body, Understanding the needs of Sukh and Suvidha; Understanding the Body as an Instrument of the Self, Understanding the characteristics and activities of self and harmony in self; Understanding the harmony of the Self with the Body, Programs to ensure self-regulation and Health

Module- 3 **5 Hours**

Understanding Harmony in the Family and Society: Harmony in the Family – the Basic Unit of Human Interaction; Understanding values in human-human relationship - meaning of Nyaya and program for its fulfillment to ensure Ubhay-tripti; 'Trust' – the Foundational Value of Relationship, Understanding the meaning of Vishwas - difference between intention and competence; Understanding the meaning of Samman - difference between respect and differentiation, the other salient values in relationship; Understanding the harmony in the society (society being an extension of family): Samadhan, Samridhi, Abhay, Sah-astitva as comprehensive Human Goals; Visualizing a universal harmonious order in society- Undivided Society (Akhand Samaj), Universal Order (Sarvabhaum Vyawastha)- from family to world family!

Module- 4 **5 Hours**

Understanding Harmony in the Nature/Existence: Understanding the harmony in the Nature; Interconnectedness and mutual fulfillment among the four orders of nature - recyclability and self-regulation in nature; Understanding Existence as Co-existence (Sah-astitva) of mutually interacting units in all-pervasive space; Holistic perception of harmony at all levels of existence.

Module- 5 **5 Hours**

Implications of the Holistic Understanding – a Look at Professional Ethics: Natural Acceptance of Human Values, Definitiveness of (Ethical) Human Conduct; A Basis for Humanistic Education; Humanistic Constitution and Universal Human Order; Competence in Professional Ethics: Ability to utilize the professional competence for augmenting universal human order, Ability to identify the scope and characteristics of people-friendly and eco-friendly production systems, Ability to identify and develop appropriate technologies and management patterns for above production systems; Case studies of typical holistic technologies, management models and production systems; Strategy for transition from the present state to Universal Human Order: At the level of individual: as socially and ecologically

responsible engineers, technologists and managers, At the level of society: as mutually enriching institutions and organizations.

Course outcomes (Course Skill Set):

At the end of the course, students are expected to become more aware of themselves, and their surroundings (family, society, nature):

CO1: Apprehend the need of Value Education over Human aspirations (PO-6)

CO2: Assimilate Harmony over the physical needs and to overcome the self- needs for a prosperous life. (PO-6)

CO3: Recognize the need of Harmony in the Family and Society for a better World. (PO-6)

CO4: Explain the need of mutual understanding for Holistic Harmony in all the Levels of Human Existence. (PO-6)

CO5: Explain the Holistic understanding of Harmony and Professional Ethics at Individual Level and Society. (PO-6, PO-8)

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the regulations; if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours).

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Books:

1. "The Textbook: A Foundation Course in Human Values and Professional Ethics", R R Gaur, R Asthana, G P Bagaria, 2nd Revised Edition, Excel Books, New Delhi, 2010. ISBN 978- 8-174-46781-2

Reference Books:

1. B L Bajpai, 2004, Indian Ethos and Modern Management, New Royal Book Co., Lucknow. Reprinted 2008.
2. PL Dhar, RR Gaur, 1990, Science and Humanism, Commonwealth Publishers.
3. Sussan George, 1976, How the Other Half Dies, Penguin Press. Reprinted 1986, 1991
4. Ivan Illich, 1974, Energy & Equity, The Trinity Press, Worcester, and HarperCollins, USA
5. Donella H. Meadows, Dennis L. Meadows, Jorgen Randers, William W. Behrens III, 1972, limits to Growth, Club of Romes Report, Universe Books.
6. Subhas Palekar, 2000, How to practice Natural Farming, Pracheen (Vaidik) Krishi Tantra Shodh, Amravati.
7. A Nagraj, 1998, Jeevan Vidya ek Parichay, Divya Path Sansthan, Amarkantak.
8. E.F. Schumacher, 1973, Small is Beautiful: a study of economics as if people mattered, Blond & Briggs, Britain.
9. A.N. Tripathy, 2003, Human Values, New Age International Publishers.

Web links and Video Lectures (e-Resources):

1. https://www.youtube.com/channel/UCQxWr5QB_eZUnwxSwxXEkQw
2. https://www.youtube.com/watch?v=P4vjfE-YnVk&list=PLWDeKF97v9SP7wSlapZcQRrT7OH0ZlGC4
3. **Course handouts:** https://drive.google.com/drive/folders/1zioX_4L2fCNX4Agw282PN86pcZZT3 Osr?usp=sharing
4. **Presentation slides:** https://drive.google.com/drive/folders/1rMUKh1s0HPRBlpp_b1mpS-duNRcwS6YH?usp=sharing