CBCS SCHEME

USN | | | | | | | | | | |

21CS33

Third Semester B.E. Degree Examination, June/July 2024
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With a neat circuit diagram and mathematical analyses explain voltage divider bias circuit. **(10 Marks)**

b. With a neat circuit diagram explain the working of relaxation oscillator. **(10 Marks)**

OR

2 a. List the advantages of active filters over passive filters. **(05 Marks)**

b. Explain any two performance parameters of power supply. **(05 Marks)**

c. Explain R-2R ladder type D to A converter. **(10 Marks)**

Module-2

3 a. Simplify the following expression using K-Map and draw the logic circuit using basic gates. $F(A, B, C, D) = \sum m(7) + \sum_d(10, 11, 12, 13, 14, 15)$. **(10 Marks)**

b. Simplify the expression using Quine-McClusky method $F(A, B, C, D) = \sum m(0, 2, 3, 6, 7, 8, 10, 12, 13)$. **(10 Marks)**

OR

4 a. Using K-Map obtain SOP and POS expressions for $f(A, B, C, D) = \sum m(6, 8, 9, 10, 11, 12, 13, 14, 15)$. **(10 Marks)**

b. With example explain,
i) Map-Entered variable method
ii) Petricks method. **(10 Marks)**

Module-3

5 a. What is Hazard? With example explain static-0 and static-1 Hazards. **(10 Marks)**

b. Implement following function using 8:1 multiplexer:
$f(a, b, c, d) = \sum_m(0, 1, 5, 6, 8, 10, 12, 15)$. **(10 Marks)**

OR

6 a. Implement full adder using 3:8 decoder and NAND gates. **(10 Marks)**

b. Design 7-segment decoder using PLA. **(10 Marks)**

Module-4

7 a. What are the 3 modeling styles in VHDL? Write VHDL code for full adder using structural model. **(10 Marks)**

b. Derive the characteristics equations for D, T, SR and JK flip flops. **(10 Marks)**

OR

8 a. Draw the logic diagram of master slave JK flipflop using NAND gates and explain its working. **(10 Marks)**

b. Explain the working of SR flipflop and show how it can be used in debounce circuit. **(10 Marks)**

Module-5

9 a. What is shift register? What are the different types of shift registers? Explain 8 bit serial-in serial-out shift register. **(10 Marks)**

b. Explain the following:

i) Sequential Parity Checker

ii) Ring Counter. **(10 Marks)**

OR

10 a. Design Mod-5 synchronous counter using JK flip flop. **(10 Marks)**

b. With diagram explain parallel adder with accumulator. **(10 Marks)**

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