CBCS SCHEME

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BCS402

Fourth Semester B.E./B.Tech. Degree Examination, June/July 2024
Microcontrollers

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Explain the architecture of an arm embedded device with a neat diagram.	10	L2	CO1
	b.	How are monitor and control internal operations performed in ARM core? Explain in brief.	10	L2	CO1
		OR			
Q.2	a.	Explain memory management in ARM core. Compare cache and tightly coupled memory.	10	L2	CO1
	b.	Explain mechanism applied by ARM core to handle exception, interrupts using different vector table.	10	L2	CO1
		Module – 2			
Q.3	a.	Examine data processing instructions requirement in the manipulation of data register? Explain in brief data processing instructions.	10	L2	CO2
	b.	Explain with examples the following 32-bit instruction of ARN processor i) CMN ii) MLA iii) MRS iv) BIC v) LDR.	10	L2	CO2
		OR			
Q.4	a.	Explain the following with example : i) Stock operation ii) Swap instructions.	10	L2	CO2
	b.	Explain Branch instructions in ARM with suitable example. Demonstrate Branch instruct usage flow of execution with an example program.	10	L2	CO2
		Module – 3			
Q.5	a.	How registers are allocated to optimize the program? Develop an assembly level program to find the sum of first to integer numbers.	10	L2	CO3
	b.	How complier handles a "for loop" with variable number of iterations N and loop controlling with an example.	10	L2	CO3
		OR			
Q.6	a.	Explain the following terms with an appropriate example : i) Pointer Aliasing ii) Portability issues.	10	L2	CO3
	b.	How function calling is efficiently used by ARM through APCS with an example program.	10	L2	CO3
		Module – 4			
Q.7	a.	Explain ARM processors exception and modes with a neat diagram.	10	L2	CO4
	b.	Explain exception priorities and link register offset.	10	L2	CO4
		OR			
Q.8	a.	List ARM firmware suite features. Explain firmware execution flow and Red Hat Boot.	10	L2	CO4
	b.	Explain IRQ and Fir exception, also to enable and disable IRQ and FIQ interrupts.	10	L2	CO4
		Module – 5			
Q.9	a.	Explain basic architecture of cache memory.	10	L2	CO5
	b.	Explain process involved in main memory mapping to a cache memory.	10	L2	CO5
		OR			
Q.10	a.	Explain with diagram set associative cache. How are efficiency is measured?	10	L2	CO5
	b.	Briefly explain cache line replacement policies with an example.	10	L2	CO5

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