

Institution	EAST POINT COLLEGE OF ENGINEERING AND TECHNOLOGY				
Department	ELECTRONICS AND COMMUNICATION ENGINEERING				
Event Type / Theme Please Tick appropriate one (v)	Club Activities/ Industrial Visit/ Guest Lecture/ Invited Talk/ Workshop / FDP /Seminar / Webinar / Conference /Sports Event /NSS Activity / Cultural Event Others (Please Mention): Webinar				
Event Title	Low Power Design Verification using System Verilog				
Date	28.09.2024		Time	2:00 PM	
Venue	Online				
Duration	<u>2 Hr</u>	From:	2:00 PM	To:	04.00PM
Program Objective	The main objective of this talk was to discuss – ASIC (Application Specific Integrated Circuit) Design flow, Digital Design Process, Verification Process, System Verilog TB Architecture, Memory DUT.				
<p>The speaker first explained the ASIC Design Flow with emphasis on its various design cycles. He then explained in detail about the chip architecture and the Digital Design Process. The students then understood the complete design of the AMBA APB based UART. We then got the complete knowledge about the verification process. Later a brief overview of the IP Verification process was dealt with. We also understood the Functional Verification at different stages of an ASIC. Different topics like Simulation and Debug, Automation, Test Plan etc. were detailed to the students. The students were then detailed about the System Verilog Architecture with emphasis on the Memory Test Bench.</p>					
1. Names of the Resource Persons / Chief Guests / Guests of Honors / Other's Mention			Mr. V Naneethakrishnan		
2. Designation/s			Senior Application Engineer		
3. Company's Name / Associations			Entuple Technologies Pvt Ltd		
Total Number of Participants			116		
Total number of Participants in <i>Google</i> Meet			116		
Total number of feedbacks received through Google forms from both Google meet and You Tube					
Total Number of Views (First Day) in YouTube			NA		

Photos

EAST POINT COLLEGE OF ENGINEERING & TECHNOLOGY
ACCREDITED BY NATIONAL BOARD OF ACCREDITATION (NBA) - CSE, ECE & ISE
Department of Electronics and Communication Engineering
Cordially Invite You To
TECHNICAL TALK ON
'Low power Design Verification Using System Verilog'

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VENUE	DATE	TIME
ECE SEMINAR HALL	28 th Sep, 2024	02:00 PM

abhyantha Memory Test bench - Program block(test) **ENTUPLE** TECHNOLOGIES

Top test bench: memory_tb

Virtual Interface: Mem_gen → gen2drv → Mem_drv → test

Physical Interface: test → Memory Controller from DUT

program: mem_test Module: memory

- All the components like generator, driver, monitor, scoreboard are constructed and connected appropriately
- All tasks for test vector generation and applying are called

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abhyantha ASiC Design flow **ENTUPLE** TECHNOLOGIES

Architecture → Functional Verification → Design → Synthesis → Design → Verification

abhyantha AMBA APB based UART Design block **ENTUPLE** TECHNOLOGIES

UART Controller, Peripheral blocks, APB, AMBA

abhyantha IP Verification **ENTUPLE** TECHNOLOGIES

IP blocks → Integration → Verification → Design → Synthesis → Design → Verification

abhyantha System Verilog RT Architecture **ENTUPLE** TECHNOLOGIES

DUT → Verilog → System Verilog → RT components

Video Recording Link / YouTube Link

: (In case of virtual event)