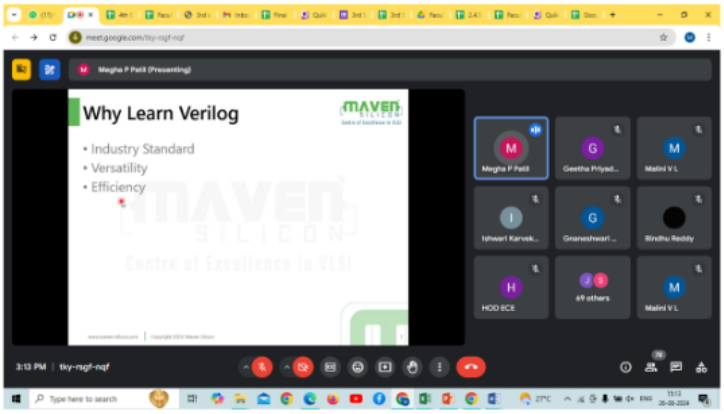
Institution	EAST POINT COLLEGE OF ENGINEERING AND TECHNOLOGY			
Department	ELECTRONICS AND COMMUNICATION ENGINEERING			
Event Type / Theme **Please Tick (√) appropriate one**	Club Activities/ Industrial Visit/ Guest Lecture/ Invited Talk/ Workshop / FDP /Seminar / Webinar / Conference /Sports Event /NSS Activity / Cultural Event Others (Please Mention): **Webinar**			
Event Title	**Leveraging Verilog for High Performance Digital System Design**			
Date	26.08.2024		Time	3:00 PM
Venue	**East Point College of Medical Science and Research Center**			
Duration	1 Hr	From: 3:00 PM	To:	04.00PM
Program Objective	To provide a deep understanding of Verilog and its application in digital system design. To demonstrate the use of Verilog in designing and simulating high-performance digital systems. To offer hands-on experience with Verilog tools and techniques, enabling participants to implement complex digital designs. To discuss the latest trends and challenges in digital system design and how Verilog can address them.			

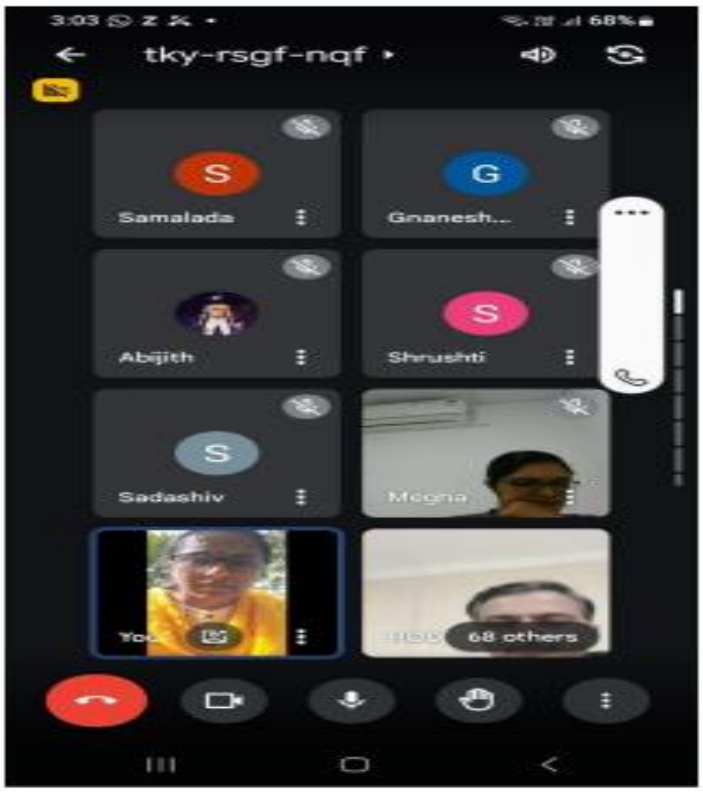
In the session the resource person introduced participants to Verilog, covering its syntax, structure, and basic concepts. Ms. Megha Patil provided a comprehensive overview of hardware description languages (HDLs) and their role in digital design. Participants were familiarized with Verilog modules, data types, and operators, laying the foundation for more advanced topics.

1. Names of the Resource Persons / Chief Guests / Guests of Honors / Other's Mention	Ms. Medha Patil
2. Designation/s	Senior Technical Faculty
3. Company's Name / Associations	Maven Silicon VLSI Training Centre
Total Number of Participants	126
Total number of Participants in *Google* Meet	
Total number of feedbacks received through Google forms from both Google meet and You Tube	
Total Number of Views (First Day) in YouTube	NA

Photos


EAST POINT COLLEGE OF ENGINEERING & TECHNOLOGY
ACCREDITED BY NATIONAL BOARD OF ACCREDITATION (NBA) - CSE, ECE & ISE
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
WEBINAR
On
LEVERAGING VERILOG FOR HIGH PERFORMANCE DIGITAL SYSTEM DESIGN
KEYNOTE SPEAKER
Ms. Megha Patil
Senior Technical Faculty
Maven Silicon VLSI Training Center
Prof. Malini V L
Faculty Co Ordinator
Dr. Yogesh G S
Vice-Principal & HOD ECE
Dr. Mrityunjaya V Latta
Principal, EPCET
DATE
26.08.2024
TIME
3.00 pm


Why Learn Verilog
• Industry Standard
• Versatility
• Efficiency
MAVEN SILICON

	
Video Recording Link / YouTube Link	: (In case of virtual event)