Institution	EAST POINT COLLEGE OF ENGINEERING AND TECHNOLOGY				
Department	ELECTRONICS AND COMMUNICATION ENGINEERING				
Event Type / Theme **Please Tick (√) appropriate one**	ClubActivities/IndustrialVisit/Guest Lecture/InvitedTalk/Workshop/FDP/Seminar / Webinar / Conference /Sports Event /NSS Activity / Cultural EventOthers(PleaseMention): Webinar				
Event Title	Introduction to FPGA Families & VIVADO Design flow				
Date	01.03.2024		Time	11:00 AM	
Venue	**ECE Class room**				
Duration	01Hrs	**From:**	11:00 AM	**To:**	**12.00PM**
Program Objective	The program objective for an Introduction to FPGA families and VIVADO Design flowwo with a thorough understanding of the basics of FPGA families,Vivado Design Flow, Imple RTL design and covering various aspects from design tohardware implementation.				

All the students were able to understand Basics of FPGA families, Vivado Design Flow, Implementing Design, Synthesizing RTL design and covering various aspects from design to hardware implementation.

1.Namesof the Resource Persons/Chief Guests /Guests of Honors/Other's Mention	**Mr. Vishnudev R Gowda**
2.Designation/s	Application Engineer
3.Company'sName/Associations	CoreEL Technologies
Total Number of Participants	103
Total number of Participants in *Google* Meet	NA
Total number of feedbacks received through Google forms from both Google meet and YouTube	NA
Total Number of Views(First Day)in YouTube	NA
Photos	

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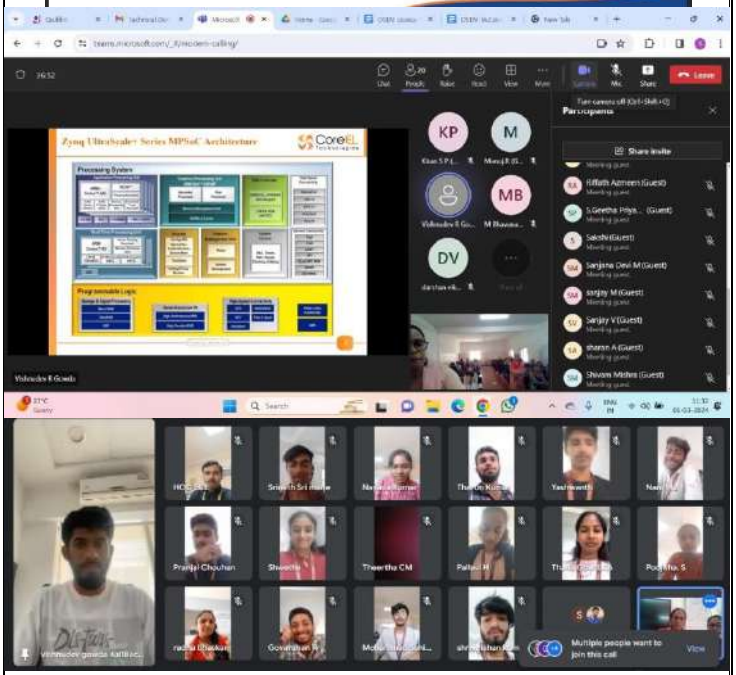
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<tr><td>Video Recording Link/YouTube Link</td><td>:(Incaseofvirtualevent)</td></tr>
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