M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER -I

ASIC DESIGN			
Course Code	22LVS12	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 10-12 Lab slots	Total Marks	100
Credits	04	Exam Hours	3

Course objectives:

- To learn ASIC methodologies and programmable logic cells to implement a function on IC.
- To Analyse back-end physical design flow, including partitioning, floor-planning, placement, and routing.
- To Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs.

MODULE-1	
Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. **CMOS Logic:** Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carryselect, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.	
Teaching-Learning Process	Chalk and talk/Power point presentation

MODULE-2	
ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages, library cell design. **Programmable ASIC Logic Cells:** MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA:XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block.	
Teaching-Learning Process	Chalk and talk/Power point presentation

MODULE-3	
Low-level design entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener. **ASIC Construction:** Physical Design, CAD Tools System partitioning, Estimating ASIC size. **Partitioning:** Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.	
Teaching-Learning Process	Chalk and talk/Power point presentation

MODULE-4	
Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. **Placement:** Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.	
Teaching-Learning Process	Chalk and talk/Power point presentation

MODULE 5	
Routing: Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back-annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.	
Teaching-Learning Process	Chalk and talk/Power point presentation

PRACTICAL COMPONENT OF IPCC.

Sl.NO	Experiments
	Develop and verify a verilog code, exercise a testbench, synthesize, and do the initial timing verification with gate level simulation. Experiments to be done using suitable CAD tools. For the set of experiments listed below, students can make the following flow as a study: - Core Constrained flow - Creation of I/O pad frame - Use the created I/O pad frame for Pad constrained design. - CTS flow Only for designs which have clock
1	Inverter
2	4-bit binary comparator composed of 2-bit comparators
3	3:8 decoder
4	Flip flop - RS, D, JK, MS, T
5	4-bit counter [Synchronous & Asynchronous counter]
6	4·bit universal shift register
7	4-bit adder/subtractor
8	12-bit register that stores an unsigned integer value

- To learn the basic science underlying individual process steps.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

1. Two Tests each of **20 Marks**
2. Two assignments each of **10 Marks/One Skill Development Activity of 20 marks**
3. Total Marks of two tests and two assignments/one Skill Development Activity added will be CIE for 60 marks, marks scored will be proportionally scaled down to **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The**15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test at the end /after completion of all the experiments shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of

IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

1. The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50 marks.
2. The question paper will have ten questions. Each question is set for 20 marks.
3. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
4. The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component).

- The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.
- SEE will be conducted for 100 marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of 50% of maximum marks of the course(CIE+SEE)

Suggested Learning Resources:

Books

1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional, 2005
2. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", Addison Wesley/ Pearson education 3rdedition, 2011
3. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, ISBN: 978-1-4614-1119-2. 2011
4. Rakesh Chadha, Bhasker J, "An ASIC Low Power Primer", Springer, ISBN: 978-14614-4270-7.

5.Peter J. Ashenden Digital Design (Verilog): An Embedded Systems Approach Using Verilog,1st Edition, Kindle Edition

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/watch?v=oZSv68esbgI
- https://www.youtube.com/watch?v=4cPkr1VHu7Q
- https://nptel.ac.in/courses/106105161

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Real world Problem Solving: Applying the ASIC front end and back end concepts.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Describe the concepts of ASIC design methodology, data path elements, logical effort .	L 1, L2
CO2	Analyze the design of ASICs suitable for specific tasks, perform design entry and explain the physical design flow.	L2,L3
CO3	Design data path elements for ASIC cell libraries and compute optimum path delay.	L3
CO4	Create floor plan including partition and routing with the use of CAD algorithms	L3, L4
CO5	Design CAD algorithms and explain how these concepts interact in ASIC design.	L2, L3

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SEMESTER -I

ADVANCED EMBEDDED SYSTEMS 1			
Course Code	22LVS13	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40Hours Theory + 10 -12 slots for Skill Development Activities	Total Marks	100
Credits	04	Exam Hours	

Course Learning objectives:

- To understand basic concepts of Embedded Systems.
- To know development of Hardware Software co-design in Embedded System.
- To understand Architecture of ARM-32 bit Microcontroller.
- To analyse Instruction sets by Assembly basics, Instruction list and description.
- To learn Cortex-M3 programming using C language concepts and Microcontroller Software Interface Standard concepts.

Module-1	
Embedded System: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-2	
Embedded System (Continued): Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-3	
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence .	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-4	
Instruction Sets: Assembly basics, Instruction list and description, useful instructions, **Memory Systems:**Memory maps, Memory access attributes ,Default Memory Access Permissions ,Bit band operations ,Endian Mode .	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-5	
Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS .	
Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Books

1. K. V. Shibu , "Introduction to embedded systems", TMH education Pvt. Ltd. 2009
2. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier) 2nd edn, 2010.
3. James K. Peckol , "Embedded systems - A contemporary design tool", John Wiley, 2008

Web links and Video Lectures (e-Resources):

- https://youtu.be/GaZBpY9Ys1Y
- https://youtu.be/SUusup7FfJo
- https://youtu.be/dHsHP9RrXBw?list=PLJ5C_6qdAvBH-JNRIlupFb44miyx9M8JD
- https://youtu.be/vn7aT9-cYzQ
- https://youtu.be/-rWGzFDLnAY

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.	L2
CO2	Explain the hardware software co-design and firmware design approaches.	L5
CO3	Understand the suitability of the instruction sets of ARM processors to design of embedded systems.	L2
CO4	Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32-bit microcontroller including memory map, interrupts and exceptions.	L5
CO5	Apply the knowledge gained for Programming ARM CORTEX M3 for different applications	L3

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
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SEMESTER -I

DIGITAL VLSI DESIGN			
Course Code	22LVS14	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours Theory + 10 -12 slots for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	3

Course Learning objectives:

- To understand the operation of MOS transistor, Scaling and Small Geometry Effects.
- To study Static Characteristics, Switching Characteristics and Interconnect Effect of MOS Inverter.
- To provide the insight of Semiconductor Memories, Dynamic Logic Circuits and BiCMOS Logic Circuits.

Module-1	
MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects. **MOS Inverters-Static Characteristics**: Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load.	
Teaching-Learning Process	Chalk and talk/Power point presentation
Module-2	
MOS Inverters-Static Characteristics: CMOS Inverter. **MOS Inverters**: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.	
Teaching-Learning Process	Chalk and talk/Power point presentation
Module-3	
Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM)	
Teaching-Learning Process	Chalk and talk/Power point presentation
Module-4	
Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS circuits	
Teaching-Learning Process	Chalk and talk/Power point presentation
Module-5	
BiCMOS Logic Circuits: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits,BiCMOS Applications.	
Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

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Suggested Learning Resources:

Books

1. "Sung Mo Kang & Yusuf Leblebici", CMOS Digital Integrated Circuits: Analysis and Design, Tata McGraw-Hill, Third Edition.
2. "Neil Weste and K. Eshraghian", Principles of CMOS VLSI Design: A System Perspective Pearson Education (Asia) Pvt. Ltd. Second Edition, 2000.
3. "Wayne, Wolf", Modern VLSI Design: System on Silicon, Prentice Hall PTR/ Pearson Education Second Edition, 1998.
4. "Douglas A Pucknell& Kamran Eshraghian", Basic VLSI Design PHI 3rd Edition

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/watch?v=57uTCtSQV50&list=PLHO2NKv71TvsSqYwVvUCZwNkY-jUyUHdS
- https://www.youtube.com/watch?v=oL8SKNxEaHs&list=PLLy_2iUCG87Bdulp9brz9AcvW_TnFCUmM

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.	L4
CO2	Analyse the Switching Characteristics in Digital Integrated Circuits.	L4
CO3	Use the Dynamic Logic circuits in state-of-the-art VLSI chips.	L3
CO4	Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon	L2
CO5	Use Bipolar and Bi-CMOS circuits in very high speed design.	L3

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
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SEMESTER -I

VLSI TESTING			
Course Code	22LVS15	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 hours Theory + 10-12 slots for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To know the various types of faults in VLSI based digital circuits.
- To examine various techniques available for efficient fault detection in combinational circuits.
- To learn the techniques to enhance testability of combinational circuits.
- To learn various techniques that can be used to make sequential circuits easily testable.

To understand test generation and response evaluation techniques used in BIST schemes for VLSI Chips.

Module-1	
Faults in digital circuits: Failures and Faults, Modeling of faults, Temporary Faults. **Logic Simulation**: Applications, Problems in simulation based design verification, types of simulation, The unknown logic values, compiled simulation, event-driven simulation, Delay models, Element evaluation, Hazard Detection, Gate-level event-driven Simulation	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-2	
Test generation for Combinational Logic circuits: Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits, Detection of multiple faults in Combinational logic circuits.	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-3	
Testable Combinational logic circuit design: Testable design of multilevel combinational circuits, Synthesis of random pattern testable combinational circuits, Path delay fault testable combinational logic design, Testable PLA design.	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-4	
Design of testable sequential circuits: Controllability and observability, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits, the scan-path technique for testable sequential circuit design, Level Sensitive Scan Design (LSSD), Random Access Scan Technique, Partial scan, testable sequential circuit design using Non scan Techniques, Cross check, Boundary Scan. .	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-5	
Built-In Self Test: Test pattern generation for BIST, Output response analysis, Circular BIST, BIST Architectures.	
Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

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Suggested Learning Resources:

Books

1. Lala Parag K," Digital Circuit Testing and Testability New York", Academic Press 1997 .
2. Abramovici M, Breuer M A and Friedman A "Digital Systems Testing and Testable Design" D Wiley 1994.
3. Vishwani D Agarwal" Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits" Springer 2002.
4. Wang, Wu and Wen Morgan" VLSI Test Principles and Architectures" Kaufmann, 2006.

Web links and Video Lectures (e-Resources):

1. https://www.youtube.com/watch?v=O5lyBoWR-PA&list=PLx98Qgh5zPjh6oWI73QfQHZAmAiyt8Wkf
2. https://www.youtube.com/watch?v=Abld-fSxjNM&list=PLbMVogVj5nJTClnafWQ9FK2nt3cGG8kCF
3. https://www.youtube.com/watch?v=MEaMm423t0w&list=PLZjlBaHNchvOFBWBAtAP9exwQgYpKqsO4&index=1
4. VTU e-learning Resources.

Skill Development Activities Suggested

2. Interact with industry (small, medium, and large).
3. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
4. Involve in case studies and field visits/ fieldwork.
5. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
6. Handle advanced instruments to enhance technical talent.
7. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
8. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical

Course outcome (Course Skill Set)		
Sl. No.	**Description**	**Blooms Level**
CO1	Analyze the need for fault modelling and testing of digital circuits	L4
CO2	Generate fault lists for digital circuits and compress the tests for efficiency	L6
CO3	Apply the various techniques to enhance testability of combinational circuits	L3
CO4	Apply boundary scan technique to validate the performance of digital circuits	L3
CO5	Design built-in self-tests for complex digital circuits	L6

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)SEMESTER -I

VLSI & ES Lab-1

Course Code	22LVSL17	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	1:2:0	SEE Marks	50
Total Hours of Pedagogy	-	Total Marks	100
Credits	02	Exam Hours	03

Sl. No	Experiments
	Part – A: VLSI Digital Design Experiments to be done using suitable CAD tools & FPGA/CPLD Boards .
	FPGA DIGITAL DESIGN VLSI Front End Design programs: Programming can be done using any compiler. Down load the programs on FPGA/CPLD boards and usepattern generator (32 channels and logic analyzer)/Chipscope pro apart from verification by simulation 1. Write Verilog code for the design of 8-bit i. Carry Ripple Adder ii. Carry Look Ahead adder iii. Carry Skip Adder 2. Write Verilog Code for 8-bit i. Array Multiplication (Signed and Unsigned) ii. Booth Multiplication (Radix-4) 3. Write Verilog code for 4/8-bit i. Magnitude Comparator ii. LFSR iii. Parity Generator 4. Develop a Verilog model for a thermostat that has two 8-bit unsigned binary inputs representing the target temperature and the actual temperature in degrees Fahrenheit (˚F). Assume that both temperatures are above freezing (32˚F). The detector has two outputs: one to turn a heater on when the actual temperature is more than 5˚F below target, and one to turn a cooler on when the actual temperature is more than 5˚F above target. 5. Develop a Verilog model of the 7-segment decoder, exercise a testbench ,synthesize and do the initial timing verification with gate level simulation. 6. Develop a Verilog model of a debouncer for a pushbutton switch that uses a debounce interval of 10ms. Assume the system clock frequency is 50MHz. 7. Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence. Eg 11101 (with andwithout overlap) any sequence can be specified.
	Part – B: Experiments to be done using ARM Cortex M3
	ARM Cortex M3 Programs - Programming to be done using suitable CAD tool and download the programon to a M3 evaluation board . a) Write an Assembly language program to calculate the sum and display the result for the addition of firstten numbers. SUM = 10+9+8+. +1
	b) Write an Assembly language program to store data in RAM c) Write a C program to output the “Hello World” message using UART d) Write a C program to operate a buzzer using Cortex M3 e) Write a C program to display the temperature sensed using Cortex M3. f) Write a C program to control stepper motor using Cortex M3.

Course outcomes:

At the end of the course the student will be able to:

1. Understand the features of CAD tool in VLSI design.
2. Design and verify the behavior of digital circuits using digital flow
3. Verify the design using a logic analyzer
4. Analyse physical design
5. Develop Assembly language programs and C language programs for different applications using ARM-Cortex M3 Kit and Keil uVision-4 tool.

Conduct of Practical Examination:

All laboratory experiments are to be included for practical examination.
For examination, one experiment from Part-A and One experiment from Part-B is to be set.
Students are allowed to pick one experiment from the lot.
Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
Change of experiment is allowed only once and Marks allotted to the Procedure part to be made zero.

Reference book : Peter J. AshendenDigital Design (Verilog): An Embedded Systems Approach Using Verilog 1st Edition, Kindle Edition

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M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER –II

Design of Analog and Mixed Mode VLSI Circuits

Course Code	22LVS21	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours Theory +10 - 12 sessions of Skill Development Activities.	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To understand the basic physics and operation of MOS devices.
- To study Single-Stage and Differential Amplifiers.
- To learn Data Converter Specifications and Architectures.
- To understand Single ended Differential Amplifier and operations.
- To learn architecture of Data converter includes ADC (Analog to Digital) and DAC(Digital to Analog) Converters.

Module-1

Basic MOS Device Physics: General considerations, MOS I/V Characteristics, second order effects, MOS device models.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-2

Single stage Amplifier: Basic Concepts, Common Source stage, Source follower.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-3

Single stage Amplifier: common-gate stage, Cascode Stage, choice of device models.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-4

Differential Amplifiers: Single ended and differential operation, Basic differential pair, Common moderesponse, Differential pair with MOS loads, Gilbert cell.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-5

Data Converter Architectures: DAC & ADC Specifications, Current Steering DAC, Charge Scaling DAC, Flash ADC, Successive Approximation ADC.

Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1) Three Unit Tests each of **20 Marks**
2) Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

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CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1) The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2) The question paper will have ten full questions carrying equal marks.
3) Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4) Each full question will have a sub-question covering all the topics under a module.
5) The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Books

1) "Behzad Razavi", Design of Analog CMOS Integrated Circuits, TMH 2007.
2) "R. Jacob Baker", CMOS Circuit Design, Layout, and Simulation, Wiley Second Edition
3) "Phillip E. Allen, Douglas R. Holberg", CMOS Analog Circuit Design Oxford University Press Second Edition.

Web links and Video Lectures (e-Resources):

1. https://www.youtube.com/watch?v=Q3WYZF5wzgU&list=PLbMVogVj5nJQB44z6h0XO2644Vbv7OM8
2. https://www.youtube.com/watch?v=311XkpNGs8c&list=PL3pGy4HtqwD0rl7gQoESHR-chSq4OPN5p
3. https://www.youtube.com/watch?v=eLTpf_5di2o&list=PLbMVogVj5nJRlMz5diOg9wBizaU6-egJc
4. https://www.youtube.com/watch?v=dcCj_xAXm4k&list=PLLDC70psjvq5vtrb0EdII4xIKA15ec-Ij
5. VTU e-learning Resources.

Skill Development Activities Suggested:

1) Interact with industry (small, medium, and large).
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities,

Course outcomes

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Use efficient analytical tools for quantifying the behaviour of basic circuits by inspection.	L2, L3
CO2	Design high-performance, amplifier circuits with the trade-offs between speed, precision and power dissipation.	L3, L4
CO3	Design and study the behaviour of phase-locked-loops for the applications.	L3,L4
CO4	Identify the critical parameters that affect the analog and mixed-signal VLSI circuits' performance	L3
CO5	Perform calculations in the digital or discrete time domain, more sophisticated data converters to translate the digital data to and from inherently analog world.	L5

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M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER -II

Advanced Embedded Systems 2			
Course Code	**22LVS22**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 10-12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course Learning objectives:

- To understand the Advanced Programming features in ARM Cortex-M3 microcontrollers
- To understand brief History of Real-Time System and Resources.
- To know Scheduler concepts and timing diagram.
- To examine various types of Memory of Real Time and I/O.

MODULE-1

Exception Programming: Using Interrupts , exception/Interrupt handlers ,software Interrupts , example of Vector Table relocation, Using SVC ,SVC example: Use for Text Message Output Functions ,Using SVC with C .

Advanced Programming Features and System Behavior: Running a system with Two separate stacks, Double-Word stack alignment, Nonbase Thread enable, Performance Considerations ,Lockup situations ,FAULTMASK .

Memory Protection unit : MPU registers ,setting Up the MPU, Typical setup **.**

Teaching-Learning Process	Chalk and talk/Power point presentation

MODULE-2

Other Cortex-M3 Features : Power Management ,Multiprocessor Communication , self-reset Control .
Debug Architecture: Debugging Features Overview ,Coresight Overview ,Debug Modes ,Debugging events ,Breakpoint in the Cortex-M3 ,accessing register Content in Debug .
Debugging Components : Trace Components: DWT,Trace Components: ITM Trace Components: eTM ,Trace Components: TpIU ,The Flash patch and Breakpoint Unit The advanced high-performance Bus access port , ROM Table
Porting Applications from the ARM7 to the Cortex-M3: System Characteristics, Assembly Language Files, C program Files.

Teaching-Learning Process	Chalk and talk/Power point presentation

MODULE-3

Real-Time Systems and Resources: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Reentrant Functions.
Processing with Real Time Scheduling: Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility

Teaching-Learning Process	Chalk and talk/Power point presentation

MODULE-4

Processing with Real Time Scheduling (Continued): Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies, Alternative to RM policy.
Memory and I/O: Worst case execution time, Intermediate I/O, ECC memory ,Multi-resource Services, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences, Reliable software, Available software.

Teaching-Learning Process	Chalk and talk/Power point presentation

MODULE 5

Firmware Components: The 3 firmware components, RTOS system software mechanisms, Debugging Components, Exceptions, assert, Checking return codes, Single-step debugging, Test access ports, Trace Ports.

Process and Threads: Process and thread creations, Programs related to semaphores, message queue, shared buffer applications involving inter task/thread communication.	
Teaching-Learning Process	Chalk and talk/Power point presentation

PRACTICAL COMPONENT OF IPCC

Sl.NO	Experiments
	Write a C Program for the following
1	To Test **4X4 keypad** using Cortex M3 microcontrollers.
2	To Display message on **Graphic LCD display** using Cortex M3 microcontrollers.
3	To Test working on Internal **ADC** using Cortex M3 microcontrollers.
4	To Test working of Internal **DAC** using Cortex M3 microcontrollers.
5	To test working of **Interrupt** using Cortex M3 microcontrollers.
6	To test on **PWM** technique using Cortex M3/M4 microcontrollers.
	Write a Assembly language program using suitable CAD software/Tools
7	To link multiple object files and link them together
8	To locking a Mutex
9	Write a SVC handler in C. Use the wrapper code to extract the correct stack frame starting location. The C handler can then use this to extract the stacked PC location and the stacked register values.
10	Write a C-program for FCFS First come first serve using suitable CAD software to Present the Output of CPU Scheduling algorithm.
11	Write a C-program for SJF Shortest job first using suitable CAD software to Present the Output of CPU Scheduling algorithm
12	Write a C-program for Priority using suitable CAD software to Present the Output of CPU Scheduling algorithm

Assessment Details (both CIE and SEE)

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CIE for the theory component of IPCC

1.Two Tests each of **20 Marks**

1. Two assignments each of **10 Marks/One Skill Development Activity of 20 marks**
2. Total Marks of two tests and two assignments/one Skill Development Activity added will be CIE for 60 marks, marks scored will be proportionally scaled down to **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The**15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test at the end /after completion of all the experiments shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

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SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

1. The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50 marks.
2. The question paper will have ten questions. Each question is set for 20 marks.
3. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
4. The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component).

- The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.
- SEE will be conducted for 100 marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of 50% of maximum marks of the course(CIE+SEE)

Suggested Learning Resources:

Books.

1. K. V. Shibu , "Introduction to embedded systems", TMH education Pvt. Ltd. 2009
2. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier) 2nd edn, 2010.
3. James K. Peckol , "Embedded systems - A contemporary design tool", John Wiley, 2008
4. Sam Siewert, Real-Time Embedded Systems and Components, Cengage Learning India Edition 2007.
5. Dr. K.V.K.K Prasad, Embedded/Real Time Systems, Concepts, Design and Programming, Black Book, , Dream Tech Press, New edition, 2010
6. James W S Liu , Real Time System, Pearson Education, 2008
7. Dream Tech Software Team , Programming for Embedded Systems, John Wiley, India Pvt. Ltd., 2008

Web links and Video Lectures (e-Resources):

- **ARM Architecture Fundamentals – https://youtu.be/7LqPJGnBPMM**
- **https://www.youtube.com/watch?v=cP6NxivTY94&list=PLbMVogVj5nJRDS4w20GO7l4SepLhuAj9 X&index=17**
  https://www.youtube.com/watch?v=Kju5UMLC7hg

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Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Real world Problem Solving: Applying the Cortex M3 Microcontroller concepts

Course outcome (Course Skill Set):

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Develop programs for real time services, firmware and RTOS, using the fundamentals of Real Time Embedded System, real time service utilities, debugging methodologies and optimization techniques.	L6
CO2	Select the appropriate system resources (CPU, I/O, Memory, Cache, ECC Memory, Microcontroller/FPGA/ASIC to improve the system performance.	L4
CO3	Apply priority based static and dynamic real time scheduling techniques for the given specifications.	L3
CO4	Analyze deadlock conditions, shared memory problem, critical section problem, missed deadlines, availability, reliability and QoS.	L4
CO5	Develop programs for multithreaded applications using suitable techniquesand data structure	L6

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
SEMESTER -II

Advances in VLSI Design			
Course Code	22LVS231	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours Theory + 10 -12 slots for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	

Course Learning objectives:

- To understand Implementation strategies for digital ICS from custom to semicustom Array Design.
- To know performance parameters of CMOS circuits,
- To learn Timing issues of digital system, Memory design and Programmable logic device (PLD).

Module-1	
Implementation Strategies For Digital ICS: Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Pre-wired Arrays, Perspective-The Implementation Platform of the Future.	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-2	
Coping With Interconnect: Introduction, Capacitive Parasitics, Capacitance and Reliability-Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability-Ohmic Voltage Drop, Electromigration, Resistance and Performance-RC Delay, Inductive Parasitics, Inductance and Reliability- Voltage Drop, Inductance and Performance-Transmission Line Effects, Advanced Interconnect Techniques,Reduced-Swing Circuits, Current-Mode Transmission Techniques, Perspective: Networks-on-a-Chip.	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-3	
Timing Issues In Digital Circuits: Introduction, Timing Classification of Digital Systems, Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design — An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock-Distribution Techniques, Latch-Base Clocking, Self-Timed Circuit Design, Self-Timed Logic - An Asynchronous Technique, Completion-Signal Generation, Self-Timed Signaling, Practical Examples of Self- Timed Logic, Synchronizers and Arbiters, Synchronizers-Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL.	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-4	
Designing Memory and Array Structures: Introduction, Memory Classification, Memory Architectures and Building Blocks, The Memory Core, Read-Only Memories, Nonvolatile Read-Write Memories, Read-Write Memories (RAM), Contents-Addressable or Associative Memory (CAM), Memory Peripheral Circuitry, The Address Decoders, Sense Amplifiers, Voltage References,Drivers/Buffers, Timing and Control.	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-5
Designing Memory and Array Structures: Memory Reliability and Yield, Signal-to-Noise Ratio, Memory yield, Power Dissipation in Memories, Sources of Power Dissipation in Memories, Partitioning of the memory, Addressing the Active Power Dissipation, Data retention dissipation, Case Studies in Memory Design: The Programmable Logic Array (PLA), A 4Mbit SRAM, A 1 Gbit NAND Flash Memory, Perspective: Semiconductor Memory Trends and Evolutions.

Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

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Suggested Learning Resources:

Books

1. Jan M Rabey, AnanthaChandrakasan, Borivoje Nikolic, "Digital Integrated Circuits-A Design Perspective", PHI, 2ndEdition
2. M. Smith, "Application Specific Integrated circuits", Addison Wesley, 1997
3. Wang, Wu and Wen, "VLSI Test Principles and Architectures", Morgan Kaufmann, 2006
4. H. Veendrick, "MOS ICs: From Basics to ASICs", Wiley-VCH, 1992

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/watch?v=kcJi8gJ1kBo&list=PLbMVogVj5nJTDr6KqQXNcxCvooSMnBuXj
- https://www.youtube.com/watch?v=ZxhaktnuBk8&list=PLbMVogVj5nJTDr6KqQXNcxCvooSMnBuXj&index=2

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical

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Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Apply design automation for complex circuits using the different implementation methodology like custom versus semi-custom, hardwired versus fixed, regular array versus ad-hoc.	L3
CO2	Use the approaches to minimize the impact of interconnect parasitics on performance, power dissipation and circuit reliability	L5
CO3	Impose the ordering of the switching events to meet the desired timing constraints using synchronous, clocked approach.	L3
CO4	Infer the reliability of the memory	L6
CO5	Understand the role of peripheral circuitry such as the decoders, sense amplifiers, drivers and control circuitry in the design of reliable and fast memories	L2

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
SEMESTER -II

Nanoelectronics			
Course Code	**22LVS232**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours Theory + 10 -12 slots for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	

Course Learning objectives:

- To understand Overview of Nano science and engineering.
- To learn Quantum confinement in semiconductor nanostructures.
- To analyze different fabrication process and physical process.
- To understand various types of methods of measuring properties and applications of Nanoelectronics.

Module-1	
Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices,Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems.	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-2	
Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-3	
Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, and electronic density of states. **Carbon Nanostructures**: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes.	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-4	
Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, colloidal quantum dots, self-assembly techniques. .	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-5	
Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum Confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural	
Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Books

1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, "Nanoscale Science and Technology", John Wiley, 2007
2. Charles P Poole, Jr, Frank J Owens, "Introduction to Nanotechnology", John Wiley Copyright 2006, Reprint 2011.
3. Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, "Hand Book of Nanoscience Engineering and Technology", CRC press, 2003.

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/watch?v=wdNFCWLuC10&list=PLbMVogVj5nJT8RG5Q4CpsJXiGqXE6t8N1
- https://www.youtube.com/watch?v=Oq5TweDVyKQ

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
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6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Know the principles behind Nanoscience engineering and Nanoelectronics.	L2
CO2	Apply the knowledge to prepare and characterize nanomaterials.	L3
CO3	Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.	L2
CO4	Design the process flow required to fabricate state of the art transistor technology.	L6
CO5	Analyze the requirements for new materials and device structure in the future	L4

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
SEMESTER -II

Static Timing Analysis			
Course Code	22LVS233	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours Theory + 10 -12 slots for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	

Course Learning objectives:

- To understand the STA Environment and concepts.
- To know standard cell library with timing model and delay model.
- To study delay calculations and timing verification concepts of flip-flops.

Module-1

Introduction: Nanometer Designs, What is Static Timing Analysis? Why Static Timing Analysis?, Crosstalk and Noise, Design Flow, CMOS Digital Designs, FPGA Designs, Asynchronous Designs, STA at Different DesignPhases, Limitations of Static Timing Analysis, Power Considerations, Reliability Considerations

STA Concepts: CMOS Logic Design, Basic MOS Structure, CMOS Logic Gate, Standard Cells, Modeling of CMOS Cells, Switching Waveform, Propagation Delay, Slew of a Waveform, Skew between Signals, Timing Arcs and Unateness, Min and Max Timing Paths, Clock Domains, Operating Conditions

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-2

Standard Cell Library: Pin Capacitance, Timing Modeling, Linear Timing Model, Non-Linear Delay Model, Example of Non-Linear, Delay Model Lookup, Threshold Specifications and Slew Derating Timing Models - Combinational Cells, Delay and Slew Models, Positive or Negative Unate, General Combinational Block, Timing Models - Sequential Cells, Synchronous Checks: Setup and Hold, Example of Setupand Hold Checks, Negative Values in Setup and Hold Checks, Asynchronous Checks, Recovery and Removal Checks Pulse Width Checks, Example of Recovery, Removal and Pulse Width Checks, Propagation Delay, State- Dependent Models XOR,XNOR and Sequential Cells, Interface Timing Model for a Black Box, Advanced Timing Modeling, Receiver Pin Capacitance, Specifying Capacitance at the Pin Level, Specifying Capacitance at the Timing Arc Level, Output Current, Models for Crosstalk Noise Analysis, DC Current, Output Voltage, Propagated Noise, Noise Models for Two-Stage Cells, Noise Models for Multi-stage and sequential Cells, Other Noise Models, Power Dissipation Modeling, Active Power,

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-3

Interconnect Parasitics: RLC for Interconnect, Wireload Models, Interconnect Trees, Specifying Wire load Models, Representation of Extracted Parasitic, Detailed Standard Parasitic Format ,Reduced Standard Parasitic Format, Standard Parasitic Exchange Format, Representing Coupling Capacitances, Hierarchical Methodology, Block Replicated in Layout, Reducing Parasitic for Critical Nets, Reducing Interconnect Resistance, Increasing Wire Spacing, Parasitics for Correlated Nets.

Delay Calculation: Overview, Delay Calculation Basics, Delay Calculation with Interconnect, Pre-layout Timing, Post-layout Timing, Cell Delay using Effective Capacitance, Interconnect Delay, Elmore Delay, Higher Order Interconnect Delay Estimation, Full Chip Delay Calculation, Slew Merging, Different Slew Thresholds, Different Voltage Domains, Path Delay Calculation, Combinational Path Delay, Path to a Flip-flop, Input to Flip-flop Path, Flip-flop to Flip-flop Path, Multiple Paths, Slack Calculation.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-4

Configuring the STA Environment: What is the STA Environment?
Specifying Clocks, Clock Uncertainty, Clock Latency, Generated Clocks, Example of Master Clock at Clock Gating Cell Output, Generated Clock using Edge and Edge shift Options, Generated Clock using Invert Option, Clock Latency for Generated Clocks, Typical Clock Generation Scenario, Constraining Input Paths, Constraining Output

Paths, Example A, Example B, Example Timing Path Groups, Modeling of External Attributes,Modeling Drive Strengths, Modeling Capacitive Load, Design Rule Checks, Virtual Clocks,	
Teaching-Learning Process	Chalk and talk/Power point presentation
Module-5	
Timing Verification: Setup Timing Check, Flip-flop to Flip-flop Path, Input to Flip-flop Path, Input Path with Actual Clock, Flip flop to Output Path, Input to Output Path, Frequency Histogram, Hold Timing Check, Flip-flop to Flip-flop Path, Hold Slack Calculation, Input to Flip-flop Path, Flip-flop to Output Path, Flip-flop to OutputPath with Actual Clock, Input to Output Path, Multicycle Paths, Crossing Clock Domains, False Paths, Half- Cycle Paths, Removal Timing Check, Recovery Timing Check, Timing across Clock Domains, Slow to FastClock Domains, Fast to Slow Clock Domains, Half-cycle Path - Case 1, Half-cycle Path -Case 2, Fast to Slow Clock Domain, Slow to Fast Clock Domain,	
Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Books

1. J. Bhasker, R Chadha, "Static Timing Analysis for Nanometer Designs: A Practical Approach", Springer 2009

Reference Books

2. Sridhar Gangadharan, Sanjay Churiwala, "Constraining Designs for Synthesis and Timing Analysis – A Practical Guide to Synopsis Design Constraints (SDC)", Springer, 2013

3. Naresh Maheshwari and SachinSapatnekar, "Timing Analysis and Optimization of Sequential Circuits", Springer Science and Business Media, 1999

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/watch?v=KlUn2GjNOfY&list=PLYdInKVfi0Ka5c6kraib5qiCFhPWE9G6e
- https://www.youtube.com/watch?v=yYR8BzysTmM&list=PLYdInKVfi0Ka5c6kraib5qiCFhPWE9G6e&index=2

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Evaluate the delay of any given digital circuits.	L5
CO2	Prepare the resources to perform the static timing analysis using EDA tool.	L6
CO3	Prepare timing constraints for the design based on the specification.	L6
CO4	Generate the timing analysis report using EDA tool for different checks.	L5, L6
CO5	Perform verification and analyse the generated report to identify critical issues and bottleneck for the violation and suggest the techniques to make the design to meet timing	L3

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER -III

Embedded Linux System Design and Development Processing			
Course Code	**22LVS234**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours Theory + 10 -12 slots for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To understand the importance of Embedded Linux in embedded system design.
- To Gain the knowledge of Board Support Package.
- To Analyse the memory requirements for design.
- To learn the embedded drivers and kernel modules.
- To learn the porting applications from traditional RTOS

Module-1	
Introduction: History of Embedded Linux, Why Embedded Linux, Embedded Linux Versus Desktop Linux, Frequently Asked Questions, Embedded Linux Distributions, Porting Roadmap. **Getting Started:** Architecture of Embedded Linux, Linux Kernel Architecture, User Space, Linux Start-Up Sequence, GNU CrossPlatform Tool chain.	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-2	
Board Support Package: Inserting BSP in Kernel Build Procedure, Memory Map, Interrupt Management, The PCI Subsystem, Timers, UART, Power Management.	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-3	
Embedded Storage: Flash Map, MTD—Memory Technology Device, MTD Architecture, Sample MTD Driver for NOR Flash, The Flash-Mapping Drivers, MTD Block and Character Devices,Mtdutils Package, EmbeddedFile Systems, Optimizing Storage Space, Tuning Kernel Memory.	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-4	
Embedded Drivers: Linux Serial Driver, Ethernet Driver , I2C Subsystem on Linux, USB Gadgets, Watchdog Timer, Kernel Modules	
Teaching-Learning Process	Chalk and talk/Power point presentation

Module-5	
Porting Applications: Architectural Comparison, Application Porting Roadmap, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver.	
Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Books

1. P.Raghavan, Amol Lad, Sriram Neelakandan" Embedded Linux System Design And Development", Auerbach Publications, Taylor & Francis Group, 2006
2. Karim Yaghmour, Jon Masters, Gilad BenYossef, and Philippe Gerum "Building Embedded Linux Systems" O'Reilly publications, 2 nd edition

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/watch?v=9vsu67uMcko

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyse and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the embedded Linux development environment.	L1,L2
CO2	Understand and create Linux BSP for a hardware platform	L1,L2
CO3	Understand the Linux model for embedded storage and write drivers and applications for the same.	L1,L2
CO4	Understand various embedded Linux drivers such as serial, I2C, and so on.	L1,L2
CO5	Port applications to embedded Linux from a traditional RTOS	L3

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)

II Semester	**VLSI Process Technology**		
Course Code	**22LVS235**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours Theory + 10 -12 slots for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	

Course Learning objectives:

- To understand the theoretical and practical aspect of very large scale integration
- To analyse doping profiles and material properties with SOI technology.
- To learn the art of lithography with different techniques.
- To analyse plasma discharge properties and the diagnostic techniques.
- To understand implantation process and applicability of metallization scheme.

Module-1

Crystal Growth and Wafer Preparation: Introduction, Electronic-Grade Silicon, Czochralski Crystal Growing.
Epitaxy: Introduction, Vapour-Phase Epitaxy.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-2

Lithography: Introduction, Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-3

Reactive Plasma Etching: Introduction, Plasma Properties, Feature-Size Control and Anisotropic Etch Mechanisms, Other Properties of Etch Processes, Reactive Plasma-Etching Techniques and Equipment, Specific Etch Processes.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-4

Ion Implantation: Introduction, Range Theory, Implantation Equipment, Annealing, Shallow Junctions, High-Energy Implantation.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-5

Metallization: Introduction, Metallization Applications, Metallization Choices, Physical Vapor Deposition, Patterning, Metallization problems .

Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1) Three Unit Tests each of **20 Marks**
2) Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1) The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2) The question paper will have ten full questions carrying equal marks.
3) Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4) Each full question will have a sub-question covering all the topics under a module.
5) The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Books

1. S. M. Sze, **"VLSI Technology"**, McGraw-Hill, Second Edition.
2. S.K. Ghandhi, **"VLSI Fabrication Principles"**, John Wiley Inc., New York, 1994, Second Edition.

Web links and Video Lectures (e-Resources):

https://www.youtube.com/watch?v=EbWmRJeNM9w&list=PLbMVogVj5nJSkDoV3lpZpZUEnzNIRsDpl

Skill Development Activities Suggested:

1) Interact with industry (small, medium, and large).
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

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Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcomes (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the major steps in the fabrication process of VLSI circuits.	L1,L2
CO2	Illustrate particular processing steps in achieving required parameters.	L1
CO3	Apply standard engineering for different lithographic methods.	L3
CO4	Analyse the specific plasma process used in semiconductor industry	L4,L5
CO5	Apply implantation process for VLSI devices and discuss the limitations of various metallization schemes.	L3,L4

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
SEMESTER -II

II Semester	**Low Power VLSI Design**		
Course Code	**22LVS241**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours Hours Theory + 10-12 sessions for SkillDevelopment Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives:

- To study State-of-the art approaches of power estimation and reduction.
- To understand power dissipation at various levels of design

Module-1

Introduction: Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits.
Simulation power analysis: SPICE circuit simulation, Monte Carlo simulation.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-2

Circuit: Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-3

Logic: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-4

Low power Architecture & Systems: Power & performance management, switching activity reduction, flow graph transformation.
Low power memory design: Introduction, sources and reductions of power dissipation in memory subsystem.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Module-5

Algorithm & Architectural Level Methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.
Advanced Techniques: Adiabatic computation, Asynchronous circuits.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentation

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1) Three Unit Tests each of **20 Marks**
2) Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1) The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2) The question paper will have ten full questions carrying equal marks.
3) Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4) Each full question will have a sub-question covering all the topics under a module.
5) The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Books

1) Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic, 1998.
2) Jan M. Rabaey, Massoud Pedram, "Low Power Design Methodologies", Kluwer Academic, 2010.
3) Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000
4) A. P. Chandrasekaran and R. W. Broadersen, "Low power digital CMOS design", Kluwer Academic,1995.
5) A Bellamour and M I Elmasri, "Low power VLSI CMOS circuit design", Kluwer Academic,1995.

Web links and Video Lectures (e-Resources):

1. https://archive.nptel.ac.in/courses/106/105/106105034/
2. https://www.youtube.com/watch?v=TFOO1JAll2Y
3. https://www.youtube.com/watch?v=ORtlxpW_LMU

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large).
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

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Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Identify the sources of power dissipation in CMOS circuits.	L1, L2
CO2	Perform power analysis using simulation-based approaches and probabilistic analysis.	L2, L3
CO3	Use optimization and trade-off techniques that involve power dissipation of digital circuits.	L2, L3
CO4	Make the power design a reality by making power dimension an integral part of the design process.	L2, L3
CO5	Use practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments.	L3, L4

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
SEMESTER -II

SoC Design			
Course Code	22LVS242	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours Theory + 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	3

Course Learning objectives:

- To Describe the organization and implementation of the 3- and 5-stage pipeline ARM processor cores
- To Understand the needs high-level language (in this case, C) in application development
- To Know the issues involved in debugging systems in embedded processor cores and in the production testing of board-level systems.
- To learn different ARM integer cores, concept of memory hierarchy and management.

Module-1

ARM Organization and Implementation: 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface.
The ARM Instruction Set: Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B, BL), Branch, Branch with Link and exchange (BX, BLX), Software Interrupt (SWI).

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-2

The ARM Instruction Set (Continued) Data processing instructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte data transfer instruction, Half-word and signed byte data transfer instructions, Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions, General register to status register transfer instructions, Coprocessor instructions, Coprocessor data operations, Coprocessor data transfers, Coprocessor register transfers, Breakpoint instruction (BRK - architecture v5T only), Unused instruction space, Memory faults, ARM architecture

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-3

Architectural Support for High-Level Languages: Abstraction in software design, Data types, Floating-point data types, The ARM floating-point architecture, Expressions, Conditional statements ,Loops, Functions and procedures, Use of memory, Run-time environment.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-4

Architectural Support for System Development: The ARM memory interface, The Advanced Microcontroller Bus Architecture(AMBA), The ARM reference peripheral specification, Hardware system prototyping tools, The ARMulator, The JTAG boundary scan test architecture, The ARM debug architecture, Embedded Trace, Signal processing support

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-5

ARM Processor Cores: ARM7TDMI, ARM8, ARM9TDMI, ARM10TDMI, Discussion, Example and exercises.
Memory Hierarchy: Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management, Examples and exercises.

Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

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to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Books

- Steve Furber "ARM System-On-Chip Architecture" Addison Wesley, 2ndedition
- Joseph Yiu "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier) , 2nd edition, 2010.
- Sudeep Pasricha and Nikil Dutt," On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008.
- Michael Keating, Pierre Bricaud "Reuse Methodology Manual for System on Chip designs", Kluwer Academic Publishers, 2ndedition, 2008.

Web links and Video Lectures (e-Resources):

- https://www.ele.uva.es/~jesman/BigSeti/ftp/Microcontroladores/ARM/Arm%20System-On-Chip%20Architecture.pdf.

Skill Development Activities Suggested :

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

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Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Apply the 3- and 5-stage pipeline ARM processor cores and analyse the implementation issues	L3
CO2	Use the concepts and methodologies employed in designing a System- on-chip (SoC) based around a microprocessor core and in designing the microprocessor core itself.	L3
CO3	Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is.	L2
CO4	Use integrated ARM CPU cores (including Strong ARM) that incorporate full support for memory management.	L3
CO5	Analyze the requirements of a modern operating system and use the ARM architecture to address the same	L4

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
SEMESTER -II

SystemVerilog			
Course Code	22LVS243	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours Theory + 10-12 sessions of Skill Development Activities.	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To understand the concepts of Verification process.
- To know the concepts of System Verilog.
- To gain the essential knowledge to write the Verification Code.
- To learn Randomization of system Verilog.
- To examine functional coverage depending upon data sample.

Module-1	
Verification Guidelines: The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components, layered testbench.	
Teaching-Learning Process	Chalk and talk/Power point presentation
Module-2	
Data Types: Built in Data types, fixed and dynamic arrays, Queues, associative arrays, linked lists, array methods, choosing a storage type, creating new types with typedef, creating user defined structures, typeconversion, Enumerated types, constants and strings, Expression width.	
Teaching-Learning Process	Chalk and talk/Power point presentation
Module-3	
Connecting the test bench and design: Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions.	
Teaching-Learning Process	Chalk and talk/Power point presentation
Module-4	
Randomization: Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, Inline constraints, Random number functions, Common randomization problems.	
Teaching-Learning Process	Chalk and talk/Power point presentation
Module-5	
Functional Coverage: Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation.	
Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1) Three Unit Tests each of **20 Marks**
2) Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**
CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1) The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2) The question paper will have ten full questions carrying equal marks.
3) Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4) Each full question will have a sub-question covering all the topics under a module.
5) The students will have to answer five full questions, selecting one full question from each module

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Suggested Learning Resources:

Books

1) Chris Spear, "System Verilog for Verification – A guide to learning the Test bench language features", Springer Publications Second Edition, 2010.
2) Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design- A guide to using system Verilog for Hardware design and modelling", Springer Publications Second Edition, 2006.

Web links and Video Lectures (e-Resources):

1. https://www.udemy.com/course/soc-verification-systemverilog/
2. https://www.udemy.com/course/learn-system-verilog-assertions-and-coverage/

Skill Development Activities Suggested:

1) Interact with industry (small, medium, and large).
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities,

Course Outcomes (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Apply the SystemVerilog concepts to verify the design.	L3
CO2	Apply constrained random tests benches using SystemVerilog.	L3
CO3	Appreciate Functional Coverage.	L3, L4

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
SEMESTER -II

HIGH FREQUENCY GaN ELECTRONIC DEVICES			
Course Code	22LVS 244	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours Theory + 10 -12 slots for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	

Course Learning objectives:

- To understand an integrated treatment of the state of the art in both conventional (i.e., HEMT) scaling as well as unconventional device architectures suitable for amplification and signal generation
- To understand the both conventional scaled HEMTs (into the deep mm-wave) as well as unconventional approaches to address the mm-wave and THz regimes;
- To know related physics, as well as numerical simulations and experimental realizations..

Module-1

Introduction and Overview:
High Power High Frequency Transistors: A Material's Perspective: Introduction, Johnson's Figure of Merit, Output Power Figure of Merit 2, Achieving Mobile Carriers for Wide Band Gap Semiconductors, Low Field Mobility Considerations, Channel Temperature Considerations, Heterojunction Advantages

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-2

Isotope Engineering of GaN for Boosting Transistor Speeds: Introduction, Current Saturation, The Effect of Non-equilibrium LO Phonons is Twofold, Derivation of the Electron-LO Phonon Interaction Hamiltonian, Evaluating the Probability of Scattering into the LO Phonon Mode q, Evaluation of the Phonon Population in Each Mode, Calculating Velocity vs. Field Dependence, Analysis, "Creative Disorder", Summary of the Theoretical Analysis, Experimental Feasibility of Introducing Isotopic Disorder in GaN HEMTs.
Linearity Aspects of High Power Amplification in GaN Transistors: "Creative Disorder", Summary of the Theoretical Analysis, Experimental Feasibility of Introducing Isotopic Disorder in GaN HEMTs, Overview of Non-linearity and Its Impacts, Trade-Offs Against Other Metrics, Origins of Non-linearity in GaN HEMTs, Transconductance, Capacitance, Self-heating, Trapping, Large-Signal Modelling, Special Concerns for GaN, Available Models, Physically Derived Models, Circuit Models, Device-Level Design for Linearity, Linearizing the Transconductance Profile, BRIDGE FET Technology.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-3

III-Nitride Tunneling Hot Electron Transfer Amplifier (THETA):
Overview of the Chapter Analysis of Hot Electron Transport and Monte Carlo Simulation, Electron Transport Scattering Mechanisms, Monte Carlo Simulation Small Signal Models for High-Frequency Performance ,Effectof Base Thickness and Doping on β, gm, Delay Component, ft, and fmax, Effect of Emitter-Base Current Density on Delay Component, ft, and fmax , Unipolar Transport in III-Nitride Alloys, Polarization-Engineered Vertical Barriers, Leakage in Vertical AlGaN/GaN Heterojunctions, Polarization-Engineered Base-Collector Barriers, Design, Growth, Fabrication, and Characterization of THETA ,Generation I: Common-Emitter Current Gain , Ga Polar THETA with Current Gain >1, N Polar THETA Hot Electron Transport in Vertical AlGaN/GaN Heterostructures, Negative Differential Resistance in III-Nitride THETA, Generation II: Current Gain > 10 in III- Nitride HETs

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-4

Plasma-Wave Propagation in GaN and Its Applications:
Electron PlasmaWaves: Physical Origin, Drude Conductivity and Distributed Models for HEMTs, Hydrodynamic Transport Equations and Non-linear Effects, Electron PlasmaWaves in GaN Experimental Demonstration, Direct Electrical Probing, Quasi-Optical Excitation, Prospective Applications, RTD-Gated HEMT .

Numerical Simulation of Distributed Electromagnetic and Plasma Wave Effect Devices: Hydrodynamic Modeling of the 2DEG Channel ,Electrodynamic Equations (or Maxwell's Equation), Finite Difference TimeDomain (FDTD) Solution, Time-Space Discretization of HD Equations, Time-Space Discretization of Maxwell'sEquation 4 Verification Using Analytical Models and Experimental Data , Model Validation Via Analytical Method , Model Validation Via Prior Measurements 5 HEMT-Based Terahertz Emitters Using PlasmaWaveInstability , Modeling of HEMT-Based Terahertz Emitters, Full-Wave Hydrodynamic Modeling of Terahertz Emissions from an Short Channel HEMT [24], Dyakonov-Shur Instability, Instability Mechanism , Instability inUngated InGaAs HEMT,

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-5

Resonant Tunneling Transport in Polar III-Nitride:
Introduction, Background on Resonant Tunneling Devices, III-Nitride-Based Resonant Tunneling Devices, Polar Double-Barrier Heterostructures, Molecular Beam Epitaxy of III-Nitride RTDs, GaN/AlN Resonant Tunneling Diodes, Polar RTD Model,New Tunneling Features in Polar RTDs, Polar RTD at Resonance, Polarization- Induced Threshold Voltage,

Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Books

1. Patrick Fay, Debdeep Jena, Paul Maki, "High-Frequency GaN Electronic Device", Springer International Publishing, 2020

Web links and Video Lectures (e-Resources):

1. https://www.youtube.com/watch?v=BboadvgRTYI
2. https://www.youtube.com/watch?v=o3369LXjt3o

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large).
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Describe the role and impact of nitrogen isotopic selection in material growth and its impact on carrier transport for increasing device speed and power.	L2
CO2	Analyse two distinct perspectives on novel approaches for improving the linearity of GaN-based devices (a key metric for emerging high-speed communications applications) in terms of unconventional device concepts in the III-N material system.	L4
CO3	Analyse hot-carrier injection-based devices, plasma-wave-based devices, and resonant tunneling diodes.	L4
CO4	Understand the emergence of high-speed devices demands new techniques for characterization of devices and also new approaches to numerical simulation of devices.	L2
CO5	Describe emerging noncontact fabrication and characterization techniques for ultrahigh-speed devices	L5

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
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SEMESTER -II

II Semester	**Machine Learning and Deep Learning**		
Course Code	**22LVS245**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours Theory + 10-12 sessions of Skill Development Activities.	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To understand various key paradigms for machine learning approaches
- To familiarize with the mathematical and statistical techniques used in machine learning
- To understand and differentiate among various machine learning techniques
- To know technical details about various recent algorithms related to Machine Learning with specific focus on Deep Learning

Module-1

Supervised Learning - Introduction: Motivation, Different types of learning, Linear regression, Logistic regression Support Vector Machines: Hard SVM, Soft SVM, Optimality conditions, Duality, Kernel trick, Implementing Soft SVM with Kernels

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-2

Decision Trees: Decision Tree algorithms, Random forests
Neural Networks: Feedforward neural networks, Expressive power of neural networks, SGD and Backpropagation Model selection and validation: Validation for model selection, k-fold cross-validation, Training Validation-Testing split, Regularized loss minimization

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-3

Unsupervised Learning and Generative Models - Nearest Neighbour: k-nearest neighbour, Curse of dimensionality Clustering: Linkage-based clustering algorithms, k-means algorithm, Spectral clustering Dimensionality reduction: Principal Component Analysis, Random projections, Compressed sensing

Teaching-Learning Process	Chalk and talk , Power point presentation ,NPTEL ,VTU E-learning resources , Experimental learning, Problem based learning

Module-4

Foundations of Deep Learning: DNN, CNN, Autoencoders

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-5

Introduction to Deep Learning - Model Search: Optimization, Regularization, AutoML
Applications: Neural language models

Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1) Three Unit Tests each of **20 Marks**
2) Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1) The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2) The question paper will have ten full questions carrying equal marks.
3) Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4) Each full question will have a sub-question covering all the topics under a module.
5) The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Books

1) Shalev-Shwartz,S., Ben-David,S., (2014), Understanding Machine Learning: From Theory to Algorithms, Cambridge University Press
2) R. O. Duda, P. E. Hart, D. G. Stork (2000), Pattern Classification, Wiley-Blackwell, 2nd Edition
3) Goodfellow,I., Bengio.,Y., and Courville,A., (2016), Deep Learning, The MIT Press
4) Mitchell Tom (1997). Machine Learning, Tata McGraw-Hill
5) C. M. BISHOP (2006), Pattern Recognition and Machine Learning, Springer-Verlag New York, 1st Edition.
6) Charniak, E. (2019), Introduction to deep learning, The MIT Press.

Web links and Video Lectures (e-Resources):

3. Department of Computer Science, Stanford University, https://see.stanford.edu/Course/CS229
4. https://www.deeplearningbook.org/

Skill Development Activities Suggested:

1) Interact with industry (small, medium, and large).
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Formulate a machine learning problem	L1, L2
CO2	Select an appropriate pattern analysis tool for analyzing data in a given feature space	L4
CO3	Apply pattern recognition and machine learning techniques such as classification to practical applications and detect patterns in the data	L3
CO4	Design efficient algorithms related to recent machine learning techniques, train models, and develop real-world ML-based applications	L3

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)SEMESTER -III

MINI PROJECT WITH SEMINAR

Course Code	22LVS25	CIE Marks	100
Teaching Hours/Week (L:P:SDA)	0:4:2	SEE Marks	-
Total Hours of Pedagogy	-	Total Marks	100
Credits	03	Exam Hours	-

Course objectives:

- To support independent learning and innovative attitude.
- To guide to select and utilize adequate information from varied resources upholding ethics.
- To guide to organize the work in the appropriate manner and present information (acknowledging thesources) clearly.
- To develop interactive, communication, organization, time management, and presentation skills.
- To impart flexibility and adaptability.
- To inspire independence and team working.
- To expand intellectual capacity, credibility, judgment, intuition.
- To adhere to punctuality, setting and meeting deadlines.
- To instill responsibilities to oneself and others.
- To train students to present the topic of project work in a seminar without any fear, face the audience confidently, enhance communication skills, involve in group discussion to present and exchange ideas.

Mini-Project with seminar : Each student shall involve in carrying out the project work jointly in constant consultation with Internal guide, co-guide, and external guide and prepare the project report as per the norms avoiding plagiarism.

Course outcomes:

At the end of the course the student will be able to:

- Present the mini-project and be able to defend it.
- Make links across different areas of knowledge and generate, develop and evaluate ideas andinformation so as to apply these skills to the project task.
- Habituated to critical thinking and use problem-solving skills.
- Communicate effectively and to present ideas clearly and coherently in both written and oral forms.
- Work in a team to achieve a common goal.
- Learn on their own, reflect on their learning and take appropriate actions to improve it.

CIE procedure for Mini - Project:

The CIE marks awarded for Mini - Project, shall be based on the evaluation of Mini - Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25.The marks awarded for Mini - Project report shall be the same for all the batch mates.

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)SEMESTER -II

VLSI & ES Lab-2

Course Code	22LVSL26	CIE Marks	40
TeachingHours/Week (L:T:P)	0:0:4	SEE Marks	60
Credits	02	Exam Hours	03

Sl. NO	Experiments
	PART A: VLSI Design. **Experiments to be conducted using suitable CAD tool**
1	Design an Inverter with given specifications*, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) Transient Analysis b. Draw the Layout and verify the DRC, ERC c. Check for XX d. Extract RC and back annotate the same and verify the Design e. Verify & Optimize for Time, Power and Area to the given constraint***
2	Design the following circuits with given specifications*, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC, LVS c. Check for XX d. Extract RC and back annotate the same and verify the Design i) Single Stage differential amplifier ii) Common source amplifier iii) Design an op-amp with given specification* using differential amplifier Commonsource amplifier in library** iv) Design a 4 bit R-2R based DAC for the given specification**
3	Design an Integrator using OPAMP (First Order)
4	Design a Differentiator using OPAMP (First Order)
5	Design and characterize a basic Sigma delta ADC from the available designs.
	(Any other experiments may be added in supportive of the course) *Appropriate specification should be given. ** Applicable Library should be added & information should be given to the Designer. *** An appropriate constraint should be given
	PART B: RTOS programs using C language in LINUX OS.
1	Develop programs to (a) create child process and display its id and (b) Execute child process function using switch structure
2	Develop and test program for a multithreaded application, where communication is through a buffer forthe conversion of lowercase text to uppercase text, using semaphore concept.
3	Develop and test program for a multithreaded application, where communication is through sharedmemory for the conversion of lowercase text to uppercase text.
4	Develop program for inter-thread communication using message queue.Data is to be input from the keyboard for the chosen application.

5	Create 'n' number of child threads. Each thread prints the message "I'm in thread number …" and sleepsfor 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.
6	Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism.

Course outcomes:

At the end of the course the student will be able to:

1. Design, implement and analyse analog, digital and mixed mode circuits
2. Learn the various issues in Mixed signal designs basically data converters.
3. Acquire hands-on skills of using CAD tools in VLSI design and Appreciate the design process in VLSIthrough a mini-project on the design of a CMOS sub-system.
4. Implement different techniques of message passing and Inter task communication.
5. Implement different data structures such as pipes, queues and buffers in multithreaded programming and alsoselect a suitable task switching technique in a multithreaded application.

Conduct of Practical Examination:

All laboratory experiments are to be included for practical examination.For examination, two questions using different tool to be set.

Students are allowed to pick one experiment from the lot.

Strictly follow the instructions as printed on the cover page of answer script for breakup of marks. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
SEMESTER -III

CAD of DIGITAL SYSTEMS			
Course Code	22LVS31	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40Hours Theory + 10 -12 slots for Skill Development Activities	Total Marks	100
Credits	04	Exam Hours	3

Course Learning objectives:

- To learn the algorithms to design digital systems .
- To understand the optimization methods .
- To learn minimization the area of the design .
- To learn the selection of CAD problems and algorithms to solve them with simulation, logic synthesis, highlevel synthesis, and several aspects of layout design, the wide range of VLSI design automation tools .

Module-1

Introduction to Design Methodologies: The VLSI Design Problem, The Design Domains, Design Actions, DesignMethods and Technologies.
VLSI Design Automation tools: Algorithmic and System Design, Structural and Logic Design, Transistor-levelDesign, Layout Design, Verification Methods.
Algorithmic graph theory and computational complexity: Terminology, Data Structures for the Representation ofGraphs, Computational Complexity, Examples of Graph Algorithms.
Tractable and intractable problems: Decision Problems, Complexity Classes, NP-completeness and NP-hardness,

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-2

General purpose methods for combinational optimization: Backtracking and Branch-and-bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu Search, Genetic Algorithms, A Few Final Remarks on General-purpose Methods.
Layout compaction: Design Rules, Symbolic Layout, Problem Formulation, Algorithms for Constraint-graph Compaction, Other Issues.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-3

Placement and partitioning: Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithm, Partitioning.
Floor planning: Floor planning Concepts, Shape Functions and Floorplan Sizing.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-4

Routing: Types of Local Routing Problems, Area Routing, Channel Routing, Introduction to Global Routing, Algorithms for Global Routing.
Simulation: General Remarks on VlSl Simulation, Gate-level Modeling and Simulation, Switch-level Modeling andSimulation.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-5

Logic Synthesis and Verification: Introduction to Combinational Logic Synthesis, Binary-decision Diagrams, Two- level Logic Synthesis
High level synthesis: Hardware Models for High Level Synthesis, Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithm, Some Aspects of the Assignment Problem.

Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Books.

- S H Gerez Algorithms for VLSI Design Automation ,Wiley, India 2nd Edition
- N.A. Sherwani Algorithms for VLSI Physical Design Automation Springer International edition 3rd Edition

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/watch?v=FVmsr-c6g3k
- https://www.youtube.com/watch?v=gRC7C_PtfYw

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large).
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the various design methodologies.	L2
CO2	Solve graph theoretic problems.	L3 ,L5
CO3	Evaluate the computational complexity of an algorithm.	L5
CO4	Write algorithms for VLSI Automation.	L1
CO5	Simulate and synthesize digital circuits using VLSI automation tools.	L4

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER –III

FinFETs and Other Multi-Gate Transistors			
Course Code	22LVS321	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3

Course Learning Objectives:

- To learn the evolution of SOI MOS transistor.
- To have an insight into thin film formation techniques and advanced gate stack deposition.
- To enable the students to analyse physics behind BSIM-CMG.
- To analyse the electrostatics of the multi-gate MOS system.
- To realise the interrelationship between the multi-gate FET device properties and digital and analog circuits.

Module-1

he SOI MOSFET: From Single Gate to MultiGate:
brief history of Multiple - Gate MOSFETs, MultiGate MOSFET physics.

Teaching-Learning Process	Chalk and talk method/Power Point Presentation

Module-2

Multigate MOSFET Technology : Introduction, Active Area:Fins, Gate Stack

Teaching-Learning Process	Chalk and talk method/Power Point Presentation

Module-3

SIM- CMG: A Compact Model for Mult-Gate Transistors : Introduction, Framework for MultiGate FET Modeling, MultiGate Models, BSIM-CMG and BSIM-IMG, BSIM-CMG.

Teaching-Learning Process	Chalk and talk method/Power Point Presentation

Module-4

Physics of the MultiGate MOS system : Device electrostatics, Double gate MOS system, Two-dimensional confinement.

Teaching-Learning Process	Chalk and talk method/Power Point Presentation

Module-5

Multi-Gate MOSFET circuit Design : Introduction, Digital Circuit Design, Analog Circuit Design

Teaching-Learning Process	Chalk and talk method/Power Point Presentation, Demonstration of circuits.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1) Three Unit Tests each of **20 Marks**
2) Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course

Semester End Examination:

1) The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2) The question paper will have ten full questions carrying equal marks.
3) Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4) Each full question will have a sub-question covering all the topics under a module.
5) The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Books

1) J.P.Colinge,: FinFETs and other Multi-Gate Transistors, springer, Series on Integrated Circuits and Systems.
2) Samar Saha, : Fin FET Devices for VLSI Circuits and Systems, CRC Press, First Edition, 2020
3) Weihua Han,Zhiming M. Wang, : Toward Quantum FinFET , Springer Cham, First Edition 2021.
4) Yogesh singh Chauhan, Darsen D, et.al , FinFET Modeling for IC Simulation and Design: using the BSIM-CMG standard, Academic Press, 2015.

Web links and Video Lectures (e-Resources) :

1. http://www.ee.iitb.ac.in
2. http://online courses.nptel.ac.in
3. http;//icmaskdesign.com
4. http;//link.springer.com

Skill Development Activities Suggested

- Assignments
- Seminar
- Literature survey

Skill Development Activities Suggested:

1) Interact with industry (small, medium, and large).
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO 1	List out the advantages and challenges of Multi-gate Fin FETs.	L2
CO 2	Describe thin film formation technique, gate stack deposition and physics beyond BSIM-CMG.	L3
CO 3	Analyse electrostatics of multi-gate MOS system and corelate multigate FET device properties and elementary digital and analog circuits.	L3

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER -III

Internet of Things			
Course Code	22LVS322	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3

Course Learning objectives:

- To understand the concepts of IOT and its applications in today's scenario.
- To study the IoT network architecture and design.
- To Understand IOT content generation and transport through networks use cases of IoT.
- To Understand the devices employed for IOT data acquisition.

Module-1

What is IoT ?
Genesis, Digitization, Impact, Connected Roadways, Buildings, Challenges
IoT Network Architecture and Design
Drivers behind new network Architectures, Comparing IoT Architectures, M2M architecture, IoT world forum standard, IoT Reference Model, Simplified IoT Architecture.

Teaching-Learning Process	Chalk and talk , Power point presentation ,NPTEL ,VTU E-learning resources , Experimental learning, Problem based learning

Module-2

IoT Network Architecture and Design
Core IoT Functional Stack, Layer1(Sensors and Actuators), Layer 2(Communications Sublayer), Access network sublayer, Gateways and backhaul sublayer, Network transport sublayer,IoT Network management.
Layer 3(Applications and Analytics) – Analytics vs Control, Data vs Network Analytics, IoT Data Managementand Compute Stack

Teaching-Learning Process	. Chalk and talk , Power point presentation ,NPTEL ,VTU E-learning resources , Experimental learning, Problem based learning

Module-3

Engineering IoT Networks
Things in IoT – Sensors, Actuators, MEMS and smart objects.Sensor networks, WSN, Communication protocols for WSN Communications Criteria, Range, Frequency bands, power consumption, Topology, Constrained Devices, Constrained Node Networks
IoT Access Technologies, IEEE 802.15.4
Competitive Technologies – Overview only of IEEE 802.15.4g, 4e, IEEE 1901.2a Standard Alliances – LTE Cat0, LTE-M, NB-IoT

Teaching-Learning Process	Chalk and talk , Power point presentation ,NPTEL ,VTU E-learning resources , Experimental learning, Problem based learning

Module-4

Engineering IoT Networks
IP as IoT network layer, Key Advantages, Adoption, Optimization, Constrained Nodes, Constrained Networks, IP versions, Optimizing IP for IoT. Application Protocols for IoT – Transport Layer, Application Transport layer, Background only of SCADA,Generic web based protocols, IoT Application Layer
Data and Analytics for IoT – Introduction, Structured and Unstructured data, IoT Data Analytics overview and Challenges.

Teaching-Learning Process	Chalk and talk , Power point presentation ,NPTEL ,VTU E-learning resources , Experimental learning, Problem based learning

Module-5

IoT in Industry (Three Use cases)
IoT Strategy for Connected manufacturing, Architecture for Connected Factory
Utilities – Power utility, IT/OT divide, Grid blocks reference model, Reference Architecture, Primary substation grid block and automation.
Smart and Connected cities –Strategy, Smart city network architecture, Street layer, city layer, Data center layer,

services layer, Smart city security architecture, Smart street lighting.

Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

1. David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry, "Cisco, IOT Fundamentals – Networking Technologies, Protocols, Use Cases for IOT", Pearson Education; First edition 2017, ISBN: 978-9386873743.
2. Arshdeep Bahga and Vijay Madisetti, "Internet of Things – A Hands on Approach", Orient Blackswan Private Limited - New Delhi; First edition

Web links and Video Lectures (e-Resources):

1. https://archive.nptel.ac.in/courses/106/105/106105166/
2. https://www.youtube.com/watch?v=urUBLmXFKl0&list=PLgMDNELGJ1CaBrefq-0eYatfOnoncW0y-
3. https://www.youtube.com/watch?v=Yci9PfPppiw&list=PLgMDNELGJ1CZoUIF-iKcH9TSVcmG6IBcU

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large).
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the basic concepts IoT Architecture and devices employed.	L1, L2
CO2	Analyze the sensor data generated and map it to IoT protocol stack for transport.	L2, L3
CO3	Apply communications knowledge to facilitate transport of IoT data over various available communications media.	L2, L3
CO4	Design a use case for a typical application in real life ranging from sensing devices to analyzing the data available on a server to perform tasks on the device.	L3, L4
CO5	Apply knowledge of Information technology to design the IoT applications.	L3, L4

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER -III

VLSI Design for Signal Processing			
Course Code	**22LVS323**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To learn the Transformations for high speed design using pipelining, retiming, and parallel processing techniques
- To understand the Power reduction transformations for supply voltage reduction as well as for strength or capacitance reduction
- To analyse area reduction using folding techniques
- To create Strategies for arithmetic implementation
- To understand Synchronous, wave, and asynchronous pipelining

Module-1

Introduction to DSP Systems: Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms.
Iteration Bounds: Data flow graph Representations, loop bound and Iteration bound. Algorithms for ComputingIteration Bound, Iteration Bound of multi rate data flow graphs.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-2

Pipelining and Parallel Processing: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power.
Retiming: Definition and Properties, Solving Systems of Inequalities, Retiming Techniques.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-3

Unfolding: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding.
Folding: Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-4

Systolic Architecture Design: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design forspace representation containing Delays.
Fast convolution: Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-5

Pipelined and Parallel Recursive and Adaptive Filter: Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing, pipelined adaptive digital filter.

Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Books.

1. Keshab K.Parthi , VLSI Digital Signal Processing systems, Design and implementation, Wiley, 1999
2. Mohammed Isamail and Terri Fiez , Analog VLSI Signal and Information Processing, Mc Graw-Hill, 1994
3. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985
4. Jose E. France, Yannis Tsividis, Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing. Prentice Hall, 1994
5. Lars Wanhammar, DSP Integrated Circuits, Academic Press Series in Engineering, 1stEdition

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/watch?v=3UZdP-bTJtQ&list=PL3p-ZpXPqK6vvxeTp1k4kDMJj74WIetyC
- https://www.youtube.com/watch?v=BJE0wWb5HL4&list=PL3pZpXPqK6vvxeTp1k4kDMJj74WIetyC&index=2

Skill Development Activities Suggested

1) Interact with industry (small, medium, and large).
2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3) Involve in case studies and field visits/ fieldwork.
4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5) Handle advanced instruments to enhance technical talent.
6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Illustrate the use of various DSP algorithms and addresses their representation using block diagrams, signal flow graphs and data-flow graphs	L3 ,L6
CO2	Use pipelining and parallel processing in design of high-speed /low-power applications	L6
CO3	Apply unfolding in the design of parallel architecture.	L3
CO4	Evaluate the use of look-ahead techniques in parallel and pipelined IIR Digital filters.	L5
CO5	Develop an algorithm or architecture or circuit design for DSP applications	L6

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
SEMESTER -III

ADVANCES IN IMAGE PROCESSING			
Course Code	**22LVS324**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	

Course Learning objectives:

- Acquire fundamental knowledge in understanding the representationof the digital image and its properties
- Equip with some pre-processing techniques required to enhance theimage for further analysis purpose.
- Select the region of interest in the image using segmentationtechniques.
- Represent the image based on its shape and edge information.
- Describe the objects present in the image based on its properties and structure.

Module-1

The image, its representations and properties: Imagerepresentations a few concepts, Image digitization, Digital image properties, Color images.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-2

Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-3

Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-4

Shape representation and description: Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-5

Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons and object marking, Morphological segmentations and watersheds

Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Books

- Milan Sonka, Vaclav Hlavac, Roger Boyle, "Image Processing, Analysis, and Machine Vision", Cengage Learning, 2013, ISBN: 978-81-315-1883-0
- Geoff Doughertry, Digital Image Processing for Medical Applications,Cambridge university Press, 2010
- S.Jayaraman, S Esakkirajan, T.Veerakumar, Digital Image Processing,Tata McGraw Hill, 2011

Web links and Video Lectures (e-Resources):

https://www.youtube.com/watch?v=EcSvZIFIz6c
https://www.youtube.com/watch?v=RXLPYdBQRtU

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the representation of the digital image and its properties	L1
CO2	Apply pre-processing techniques required to enhance the image for its further analysis.	L1,L2
CO3	Use segmentation techniques to select the region of interest in the imagefor analysis	L1,L2,L3
CO4	Represent the image based on its shape and edge information.	L1,L2,L3
CO5	Describe the objects present in the image based on its properties andstructure.	L1,L2,L3

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (LVS)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)
SEMESTER -III

Advanced Computer Architecture			
Course Code	**22LVS325**	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives:

- To understand the advanced design principles of modern processors and parallelism.
- To learn different Pipelining & Superscalar Technologies for processors.
- To know different techniques of Parallel Programming Models, Languages & Compilers.

Module-1

Parallel Computer Models: The State of Computing, Multiprocessors and multicomputers, Multivector and SIMD computers.
Program and Network Properties: Conditions of parallelism, Program Partitioning & Scheduling, Program Flow Mechanisms.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-2

Principles of Scalable Performance: Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches.
Processors & Memory Hierarchy: Advanced processor technology, Super Scalars & Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-3

Bus, Cache and Shared Memory: Bus Systems, Cache Memory Organizations, Shared Memory Organizations, Sequential & Weak Consistency Model.
Pipelining & Superscalar Technologies: Linear Pipeline Processors, Nonlinear Pipeline Processors, InstructionPipeline Design, Arithmetic Pipeline Design, Superscalar Pipeline Design.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-4

Multivector& SIMD Computers: Vector Processing principles, Multivector Multiprocessors, Compound Vector Processing, SIMD Computer Organization.
Scalable, Multithreaded and Data Flow Computers: Latency Hiding Techniques, Principles of Multithreading, Fine Grain Multi Computers, Scalable and Multithreaded Architectures, Data Flow and Hybrid Architectures.

Teaching-Learning Process	Chalk and talk/Power point presentation

Module-5

Parallel Models, Languages and Compilers: Parallel Programming Models, Parallel Languages & Compilers, Dependence Analysis and Data Arrays, Code Optimization and Scheduling, Loop Parallelization and Pipelining.
Parallel Program Development and Environments: Parallel Programming Environments, Synchronization and Multi Processor Modes, Shared Variable Program Structures.

Teaching-Learning Process	Chalk and talk/Power point presentation

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Books

1. Kai Hwang & Narendra Jotwani, Advanced Computer Architecture: Parallelism, Scalability,Programmability, McGraw Hill Education, ISBN: 978-93-392-2092-1, 3rd Edition,2016.
2. M.J. Flynn, Computer Architecture, Pipelined and Parallel Processor Design, Narosa Publishing, 2002
3. Michael J Quinn, Parallel programming in C with MPI and OpenMP, Tata McGraw Hill, 2013
4. Ananth Grama, An Introduction to Parallel Computing: Design and Analysis of Algorithms, Pearson, 2nd Edition,2004

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/watch?v=v7iefsovo9M&list=PLwdnzlV3ogoWJhBxBYu-K4l-q-nNHd24D
- https://www.youtube.com/watch?v=4goj-ajnpOQ&list=PLwdnzlV3ogoWJhBxBYu-K4l-q-nNHd24D&index=2

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
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7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the basic concepts for parallel processing	**L2**
CO2	Analyze program partitioning and flow mechanisms	**L4**
CO3	Apply pipelining concept for the performance evaluation	L3
CO4	Learn the advanced processor architectures for suitable applications	L1
CO5	Understand parallel Programming	L2

Reconfigurable Computing		Semester	III
Course Code	22LVS331	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

This course will enable students to:

- To learn the various Reconfigurable systems.
- To study the different Languages and Compilation.
- To understand the Implementation of FPGA.
- To learn Partial Reconfiguration Design
- To understand the Signal Processing Applications

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Chalk and Talk.
2. Power Presentation and Videos.
3. Flipped Classes.
4. Practice Sessions

Module-1

troduction: History, Reconfigurable vs Processor based system, RC Architecture.

econfigurable Logic Devices: Field Programmable Gate Array, Coarse Grained ReconfigurableArrays. **Reconfigurable Computing System:** Parallel Processing on Reconfigurable Computers, A survey ofReconfigurable Computing System. (Text 1)

Module-2

Languages and Compilation: Design Cycle, Languages, HDL, High Level Compilation, Low level Design flow, Debugging Reconfigurable Computing Applications. (Text 1)

Module-3

nplementation: Integration, FPGA Design flow, Logic Synthesis.

igh Level Synthesis for Reconfigurable Devices: Modelling, Temporal Partitioning Algorithms. (Text 2)

Module-4

Partial Reconfiguration Design: Partial Reconfiguration Design, Bitstream Manipulation with JBits, The modular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, Partial Reconfiguration using Hansel-C Designs, Platform Design. (Text 2)

Module-5

gnal Processing Applications: Reconfigurable computing for DSP, DSP application building blocks, Examples: Beamforming, Software Radio, Image and video processing, Local Neighbourhood functions, Convolution. (Text 1) **System on a Programmable Chip:** Introduction to SoPC, Adaptive Multiprocessing on Chip.(Text 2)

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Understand the fundamental principles and practices in reconfigurable architecture.
2. Simulate and synthesize the reconfigurable computing architectures.
3. Understand the FPGA design principles, and logic synthesis
4. Integrate hardware and software technologies for reconfiguration computing focusing on partial reconfiguration design.
5. Design digital systems for a variety of applications on signal processing and system on chip configurations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books

1. Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays M. Gokhale and P. Graham Springer, ISBN: 978-0-387-26105-8 2005

2 . Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications C. Bobda Springer, ISBN: 978-1-4020-6088-5 2007

Reference Books

1. Practical FPGA Programming in C D. Pellerin and S. Thibault Prentice-Hall 2005

2. FPGA Based System Design W. Wolf Prentice-Hall 2004

3. Rapid System Prototyping with FPGAs: Accelerating the Design Process R. Cofer and B. Harding Newnes 2005

Web links and Video Lectures (e-Resources):

- https://in.video.search.yahoo.com/search/video;_ylt=Awrx.wZl4Ypkq6UWE__mHAx.;_ylu=c2VjA3NlYXJjaARzbGsDYXNzaXN0;_ylc=X1MDMjExNDcyMzA0NgRfcgMyBGZyA21jYWZlZQRmcjIDc2EtZ3Atc2VhcmNoBGdwcmlkA2NuaGlIRklzUi55VndlNThEcHUwV0EEbl9yc2x0AzAEbl9zdWdnAzkEb3JpZ2luA2luLnZpZGVvLnNlYXJjaC55YWhvby5jb20EcG9zAzEEcHFzdHIDTlBUIEZPUiBWSURPUyBSRUNPTkZPUkFHQUJMRSBDT01QVVRJTkcEcHFzdHJsAzM4BHFzdHJsAzQ3BHF1ZXJ5A25wdCUyMGZvciUyMHZpZGVvcyUyMHJlY29uZm9yYWdhYmxlJTIwY29tcHV0aW5nJTIwZGV2aWNlcwR0X3N0bXADMTY4NjgyMzI4MAR1c2VfY2FzZQM-?p=npt+for+videos+reconforagable+computing+devices&ei=UTF-8&fr2=sa-gp-search&fr=mcafee&type=E211IN1274G0#id=1&vid=046ac2290e69d7656fe0294da81a9091&action=view
- https://in.video.search.yahoo.com/search/video;_ylt=Awrx.waZ4YpkUqQWG.LmHAx.;_ylu=c2VjA3NlYXJjaARzbGsDYXNzaXN0;_ylc=X1MDMjExNDcyMzA0NgRfcgMyBGZyA21jYWZlZQRmcjIDc2EtZ3Atc2VhcmNoBGdwcmlkA0VPaU5zTUtGUmtlazVDSmttZ2VPcEEEbl9yc2x0AzAEbl9zdWdnAzEwBG9yaWdpbgNpbi52aWRlby5zZWFyY2gueWFob28uY29tBHBvcwMyBHBxc3RyA25wdCBmb3IgdmlkZW9zIHJlY29uZm9yYWdhYmxlIGNvbXB1dGluZwRwcXN0cmwDMzkEcXN0cmwDNDcEcXVlcnkDbnB0JTIwZm9yJTIwdmlkZW9zJTIwcmVjb25mb3JhZ2FibGUlMjBjb21wdXRpbmclMjBzeXN0ZW1zBHRfc3RtcAMxNjg2ODIzMzM2BHVzZV9jYXNlAw--?p=npt+for+videos+reconforagable+computing+systems&ei=UTF-8&fr2=sa-gp-search&fr=mcafee&type=E211IN1274G0#id=1&vid=133c016852187c2eea6cfbf3f0a28dc8&action=view

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

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Pattern Recognition & Machine Learning		Semester	III
Course Code	**22LVS332**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	**Theory**		

Course objectives:

1. To understand the model selection and different types of variables.
2. To study Supervised Learning Linear Regression Models.
3. To learn the various types of Supervised Learning Kernels.
4. To get familiar with Unsupervised Learning.
5. To learn the Probabilistic Graphical Models.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Chalk and Talk.
2. Power Presentation and Videos.
3. Flipped Classes.
4. Practice Sessions.

Module-1

troduction: Probability Theory, Model Selection, The Curse of Dimensionality, Decision Theory, Information Theory Distributions: Binary and Multinomial Variables, The Gaussian Distribution, The Exponential Family, Nonparametric Methods. (Ch.: 1,2)

Module-2

Supervised Learning Linear Regression Models: Linear Basis Function Models, The Bias-Variance Decomposition, Bayesian Linear Regression, Bayesian Model Comparison Classification & Linear Discriminant Analysis: Discriminant Functions, Probabilistic Generative Models, Probabilistic Discriminative Mode (Ch.:3,4).

Module-3

upervised Learning Kernels: Dual Representations, Constructing Kernels, Radial Basis Function Network, Gaussian Processes Support Vector Machines: Maximum Margin Classifiers, Relevance Vector Machines Neural Networks: Feed-forward Network, Network Training, Error Back propagation (Ch:5,6,7).

Module-4

Unsupervised Learning: Mixture Models: K-means Clustering, Mixtures of Gaussians, Maximum likelihood, EM for Gaussian mixtures, Alternative View of EM. Dimensionality Reduction: Principal Component Analysis, Factor/Component Analysis, Probabilistic PCA, Kernel PCA, Nonlinear Latent Variable Models (Ch.: 9,12).

Module-5

obabilistic Graphical Models: Bayesian Networks, Conditional Independence, Markov Random Fields, Inference in Graphical Models, Markov Model, Hidden Markov Models (Ch.:8,13)

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Identify areas where Pattern Recognition and Machine Learning can offer a solution.
2. Describe the strength and limitations of some techniques used in computational Machine Learning for classification, regression and density estimation problems.
3. Describe and model data.
4. Solve problems in Regression and Classification.
5. Discuss main and modern concepts for model selection and parameter estimation in recognition, decision making and statistical learning problems.

10.08.2023

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

5. The question paper will have ten questions. Each question is set for 20 marks.
6. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
7. The students have to answer 5 full questions, selecting one full question from each module.
8. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. Pattern Recognition and Machine Learning Christopher Bishop Springer 2006

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/playlist?list=PLbRMhDVUMngcx-ATexXZH_-u1wsIGIiyS
- https://www.youtube.com/watch?v=s0ZKnU-2Sps

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

-

Long Term Reliability of VLSI Systems		Semester	III
Course Code	**22LVS333**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	**Theory**		

Course objectives:

- To Understand the Various Concepts Related To Electro migration Reliability.
- To study the Fast EM Stress Evolution Analysis.
- To study the EM Assessment for Power Grid Networks.
- To understand the Transistor Aging Effects and Reliability.
- To learn the Aging Effects in Sequential Elements.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Chalk and Talk.
2. Power Presentation and Videos.
3. Flipped Classes.
4. Practice Sessions

Module-1

ectro migration Reliability: Why Electromigration Reliability?,Why system-level EM Reliability Management? Physics- based EM Modeling, Electromigration Fundamentals, Stress based EM Modeling and stress diffusion equations, Modeling for transient EM effects and Initial stress conditions, post voiding stress and void volume evolution, compact physics based EM model for a single wire, other relevant EM models and analysis methods. (Text Book:1 – 1.1, 1.2, 2.1 up to 2.6, 2.9)

Module-2

Fast EM Stress Evolution Analysis: Introduction, The LTI ordinary differential equations for EM stress evolution, The presented Krylov fast EM stress analysis, Numerical results and discussions (Text. Book:1 – 3.1 up to 3.4).

Module-3

M Assessment for Power Grid Networks: New power grid reliability analysis method, cross-layout temperature and thermal stress characterization, impact of across-layout temperature and thermal stress on EM. (Text.Book:1 – 7.1, 7.2, 7.4, 7.5).

Module-4

Transistor Aging Effects and Reliability: Introduction, Transistor reliability in advanced technology nodes, Transistor Aging, BTI- Bias Temperature Instability, HCI – Hot Carrier Injection, Coupling models for BTI and HCI degradations, RTN – Random Telegraph Noise, TDDB – Time Dependent Dielectric Breakdown. (Text Book: 1 – 13.1, 13.2)

Module-5

ing Effects in Sequential Elements: Introduction, Background: flip flop timing analysis, process variation model, voltage droop model, Robustness analysis, reliability-aware flip-flop design (Text Book: 1 – 16.1 up to 16.4).

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. At the end of the course the student will be able to:
2. Comprehend the recent research in the area of interconnect and device reliability. 2. Determine the impact of device-level reliability on system performance, built upon physics-based models.
3. Understand the physics-based EM modeling.
4. Understand the underlying phenomena of BTI, HCI, TDDB leading to device-level reliability degradation.
5. Relate to considerations at the circuit-level with both combinational and sequential elements.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

9. The question paper will have ten questions. Each question is set for 20 marks.
10. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
11. The students have to answer 5 full questions, selecting one full question from each module.
12. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1.Long-Term Reliability of Nanometer VLSI Systems Sheldon X. D. Tan, Mehdi BaradaranTahoori, Taeyoung Kim, SamanKiamehr, Zeyu Springer International Publishing 1 st Edition, 2019 ISBN: 978-3- 030-26171-9

Reference Books:

2. Reliability Wearout Mechanisms in Advanced CMOS Technologies Alvin Wayne Strong, Rolf-Peter Vollertsen, Timothy D. Sullivan, Ernest Y. Wu, Giuseppe La Rosa, Jordi Sune Wiley, Copyright © the Institute of Electrical and Electronics Engineers, Inc. 2009 Print ISBN:978047 1731726
3. Hot-carrier Reliability of MOS VLSI Circuits Yusuf Leblebici, S M Kang Springer Science & Business Media 1 st Edition, 1993
4. Fundamentals of ElectromigrationAware Integrated Circuit Design Matthias Thiele, Jens Lienig Springer

International Publishing 2018

Web links and Video Lectures (e-Resources):

- https://in.video.search.yahoo.com/search/video;_ylt=Awrx.wZyzopkCaUWKJXmHAx.?fr=mcafee&ei=UTF-8&type=E211IN1274G0&fr2=p%3As%2Cv%3Av%2Cm%3Asp-qrw-corr-top&norw=1&p=Long+Term+Reliability+of+VLSI+Systems+nptel+videos#id=6&vid=09c65429e632f047d89e3ddddbaca53b&action=view
- https://in.video.search.yahoo.com/search/video;_ylt=Awrx.wZyzopkCaUWKJXmHAx.?fr=mcafee&ei=UTF-8&type=E211IN1274G0&fr2=p%3As%2Cv%3Av%2Cm%3Asp-qrw-corr-top&norw=1&p=Long+Term+Reliability+of+VLSI+Systems+nptel+videos#id=7&vid=853453dc0d1e04a80f1416802419aa98&action=view

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

-

CMOS RF Circuit Design		Semester	III
Course Code	**22LVS334**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	**Theory**		

Course objectives:

- To Learn the RF Design, Wireless Technology and Basic Concepts.
- To understand the various Communication Concepts.
- To understand the o learn the Transceiver Architecture.
- To understand the Low Noise Amplifiers and Mixers.
- To study VCO and PLLs Oscillators.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Chalk and Talk.
2. Power Presentation and Videos.
3. Flipped Classes.
4. Practice Sessions.

Module-1

troduction to RF Design, Wireless Technology and Basic Concepts: A wireless world, RF design is challenging, The big picture. General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range, Passive impedance transformation. Scattering parameters, Analysis of nonlinear dynamic systems, conversion of gains and distortion.

Module-2

Communication Concepts: General concepts, analog modulation, digital modulation, spectral re-growth, coherent and non-coherent detection, Mobile RF communications, Multiple access techniques, Wireless standards, Appendix 1: Differential phase shift keying.

Module-3

ransceiver Architecture: General considerations, Receiver architecture, Transmitter architectures, Direct conversion and two-step transmitters, RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

Module-4

Low Noise Amplifiers and Mixers: General considerations, Problem of input matching, LNA topologies: common-source stage with inductive load, common-source stage with resistive feedback. Mixers-General considerations, passive down conversion mixers, Various mixers- working and implementation.

Module-5

O and PLLs Oscillators: Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Analyse the effect of nonlinearity and noise in RF and microwave design.
2. Exemplify the approaches taken in actual RF products.
3. Minimize the number of off-chip components required to design mixers, Low-Noise Amplifiers, VCO and PLLs.
4. Explain various receivers and transmitter topologies with their merits and drawbacks.
5. Demonstrate how the system requirements define the parameters of the circuits and the impact on the performance

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

13. The question paper will have ten questions. Each question is set for 20 marks.
14. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
15. The students have to answer 5 full questions, selecting one full question from each module.
16. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

Text Books

1. RF Microelectronics B. Razavi PHI second edition.

Reference Books:

1. CMOS Circuit Design, layout and Simulation R. Jacob Baker, H.W. Li, D.E. Boyce PHI 1998.
2. Design of CMOS RF Integrated Circuits Thomas H. Lee Cambridge University press 1998 .
3. Mixed Analog and Digital Devices and Technology Y.P. Tsividis TMH 1996.

Web links and Video Lectures (e-Resources):

- https://www.youtube.com/watch?v=oL8SKNxEaHs&list=PLLy_2iUCG87Bdulp9brz9AcvW_TnFCUmM
- https://www.youtube.com/watch?v=57uTCtSQV50&list=PLHO2NKv71TvsSqYwVvUCZwNkY-jUyUHdS

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

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Machine Learning in VLSI CAD		Semester	III
Course Code	**22LVS335**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

- To understand the Preliminary Taxonomy for Machine Learning in VLSI CAD.
- To study the Process Models and Neural Network Compact Patterning Models.
- To learn the Machine Learning for Mask Synthesis and Machine Learning in Physical Verification.
- To understand the design of Machine Learning in Mask Synthesis and Physical Design.
- To understand the Machine Learning for Yield and Reliability

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Chalk and Talk.
2. Power Presentation and Videos.
3. Flipped Classes.
4. Practice Sessions

Module-1

Preliminary Taxonomy for Machine Learning in VLSI CAD: Machine learning taxonomy, VLSI CAD Abstraction levels (Text Book:1 – 1.1, 1.2)

Machine Learning for Compact Lithographic Process Models : Introduction, Lithographic Patterning Process, Representation of Lithographic Patterning Process – Mask, Imaging, Resist & Etch Transfer Function (Text Book:1 – 2.1, 2.2).

Module-2

Machine Learning of Compact Lithographic Process Models (Cont.,) :Compact process model machine learning problem statement, CPM Task, CPM Training Experience, Performance metrics, Supervised learning of a CPM (Text. Book:1 – 2.3)

Neural Network Compact Patterning Models : Neural Network Mask Transfer Function, Neural Network Image Transfer Function, Neural Network Resist Transfer Function, Neural Network Etch Transfer Function (Text. Book:1 – 2.4).

Module-3

Machine Learning for Mask Synthesis: Introduction, Machine Learning guided OPC, MLP Construction, ML-EPC, EPC Algorithm (TextBook:1 – 3.1, 3.2, 3.2.2.2, 3.3.2, 3.3.2.4). **Machine Learning in Physical Verification**: Introduction, Machine Learning in Physical Verification – layout feature extraction & encoding, models for hotspot detection. (Text.Book:1 – 4.1, 4.2)

Module-4

Machine Learning in Mask Synthesis and Physical Design: Machine Learning inMask Synthesis – mask synthesis flow, Machine Learning for sub-resolution assist features, Machine Learning for optical proximity correction. Machine Learning inPhysical Design - for datapath placement, routability driven placement, clock optimization, lithography friendly routing (Text Book: 1 – 4.3, 4.4).

Machine Learning for Manufacturing: Gaussian Process-Based Wafer-Level Correlation Modeling and Its Applications (Text Book: 1 – 5.1).

Module-5

achine Learning for Yield and Reliability: High-volume manufacturing yield estimation – Histogram with random sampling, Histogram with GPST-PS, Kernel density estimation. (Text Book: 1 – 5.2.11).

achine learning based aging analysis (Text Book: 1 – 9.1).

arning from limited data in VLSI CAD, Iterative feature search (Text Book: 1 – 13.1, 13.2). Comparative study of

Assertion mining algorithms in GoldMine (Text Book: 1 – 20.1)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. 1. Use machine learning technologies in VLSI CAD to further automate the design, verification and implementation of the most advanced chips.
2. 2. Relate to the usage of machine learning algorithms for Compact Lithographic Process Models
3. . 3. Apply Machine Learning in Mask Synthesis and Physical Verification to bear on CAD problems such as hotspot detection, efficient test generation, post-silicon measurement minimization.
4. 4. Predict the Yield and Reliability of VLSI chips using machine learning methods. 5. Comprehend the appropriate application of the various supervised, unsupervised and statistical learning in the various layers of chip design hierarchy.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

2. The question paper will have ten questions. Each question is set for 20 marks.
3. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
4. The students have to answer 5 full questions, selecting one full question from each module.
5. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1. Machine Learning in VLSI Computer Aided Design Editors: Ibrahim (Abe)M Elfadel, Duane SBoning, Xin Li Springer International Publishing 2019

Reference Books

1. Machine Learning Tom M Mitchell McGraw-Hill 1997
2. Machine Learning Anuradha Srinivasaraghavan, Vincy Joseph Wiley 2019

Web links and Video Lectures (e-Resources):

- https://in.video.search.yahoo.com/search/video;_ylt=Awrx.wZyzopkCaUWl5TmHAx.;_ylu=c2VjA3NlYXJjaAR2dGlkAw;_ylc=X1MDMjExNDcyMzA0NgRfcgMyBGZyA21jYWZlZQRmcjIDcDpzLHY6dixtOnNiLHJnbjp0b3AEZ3ByaWQDTVpkQjZKYWJTcVdMemVFd3A4RG5IQQRuX3JzbHQDMARuX3N1Z2cDMARvcmlnaW4DaW4udmlkZW8uc2VhcmNoLnlhaG9vLmNvbQRwb3MDMARwcXN0cgMEcHFzdHJsAzAEcXN0cmwDNDAEcXVlcnkDTWFjaGluZSUyMExlYXJuaW5nJTIwaW4lMjBWTFNJJTIwQ0FEJTIwbnB0bCUyMHZpZGVvcwR0X3N0bXADMTY4NjgxODY3Mw?p=Machine+Learning+in+VLSI+CAD+nptl+videos&ei=UTF8&fr2=p%3As%2Cv%3Av%2Cm%3Asb%2Crgn%3Atop&fr=mcafee&type=E211IN1274G0#id=7&vid=cb7ebd6c1d4ee028490224221b16e987&action=view
- https://in.video.search.yahoo.com/search/video;_ylt=Awrx.wZyzopkCaUWl5TmHAx.;_ylu=c2VjA3NlYXJjaAR2dGlkAw;_ylc=X1MDMjExNDcyMzA0NgRfcgMyBGZyA21jYWZlZQRmcjIDcDpzLHY6dixtOnNiLHJnbjp0b3AEZ3ByaWQDTVpkQjZKYWJTcVdMemVFd3A4RG5IQQRuX3JzbHQDMARuX3N1Z2cDMARvcmlnaW4DaW4udmlkZW8uc2VhcmNoLnlhaG9vLmNvbQRwb3MDMARwcXN0cgMEcHFzdHJsAzAEcXN0cmwDNDAEcXVlcnkDTWFjaGluZSUyMExlYXJuaW5nJTIwaW4lMjBWTFNJJTIwQ0FEJTIwbnB0bCUyMHZpZGVvcwR0X3N0bXADMTY4NjgxODY3Mw?p=Machine+Learning+in+VLSI+CAD+nptl+videos&ei=UTF8&fr2=p%3As%2Cv%3Av%2Cm%3Asb%2Crgn%3Atop&fr=mcafee&type=E211IN1274G0#id=12&vid=1422bb4b7e46947b5b3595efd90e117f&action=view

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

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M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)SEMESTER -III

PROJECT WORK PHASE – 1

Course Code	**20LVS34**	CIE Marks	100
Number of contact Hours/Week (L:T:P)	0:0:06	SEE Marks	--
Credits	3	Exam Hours	--

Course objectives:

- Support independent learning.
- Guide to select and utilize adequate information from varied resources maintaining ethics.
- Guide to organize the work in the appropriate manner and present information (acknowledging thesources) clearly.
- Develop interactive, communication, organisation, time management, and presentation skills.
- Impart flexibility and adaptability.
- Inspire independent and team working.
- Expand intellectual capacity, credibility, judgement, intuition.
- Adhere to punctuality, setting and meeting deadlines.
- Instil responsibilities to oneself and others.
- Train students to present the topic of project work in a seminar without any fear, face audience confidently, enhance communication skill, involve in group discussion to present and exchange ideas.

Project Phase-1 Students in consultation with the guide/s shall carry out literature survey/ visit industries to finalize the topic of the Project. Subsequently, the students shall collect the material required for the selected project, prepare synopsis and narrate the methodology to carry out the project work.
Seminar: Each student, under the guidance of a Faculty, is required to

- Present the seminar on the selected project orally and/or through power point slides.
- Answer the queries and involve in debate/discussion.
- Submit two copies of the typed report with a list of references.

The participants shall take part in discussion to foster friendly and stimulating environment in which the studentsare motivated to reach high standards and become self-confident.

Revised Bloom's Taxonomy Level	L3 – Applying, L4 – Analysing, L5 – Evaluating, L6 – Creating.

Course outcomes:
At the end of the course the student will be able to:

- Demonstrate a sound technical knowledge of their selected project topic.
- Undertake problem identification, formulation and solution.
- Design engineering solutions to complex problems utilising a systems approach.
- Communicate with engineers and the community at large in written an oral forms.
- Demonstrate the knowledge, skills and attitudes of a professional engineer.

Continuous Internal Evaluation
CIE marks for the project report (50 marks), seminar (30 marks) and question and answer (20 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session bythe student) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculty from the department with the senior most acting as the Chairperson.

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)SEMESTER -III

Societal Project

Course Code	22LVS35	CIE Marks	100
Number of contact Hours/Week (L:T:P)	0:0:2	SEE Marks	--
Credits	03	Exam Hours/Batch	03

Course objectives:

- To support independent learning and innovative attitude.
- To guide to select and utilize adequate information from varied resources upholding ethics.
- To guide to organize the work in the appropriate manner and present information (acknowledging thesources) clearly.
- To develop interactive, communication, organization, time management, and presentation skills.
- To impart flexibility and adaptability.
- To inspire independence and team working.
- To expand intellectual capacity, credibility, judgment, intuition.
- To adhere to punctuality, setting and meeting deadlines.
- To instill responsibilities to oneself and others.
- To train students to present the topic of project work in a seminar without any fear, face the audience confidently, enhance communication skills, involve in group discussion to present and exchange ideas.

Mini-Project: Each student shall involve in carrying out the project work jointly in constant consultation with
internal guide, co-guide, and external guide and prepare the project report as per the norms avoiding plagiarism.

Course outcomes:

At the end of the course the student will be able to:

- Present the mini-project and be able to defend it.
- Make links across different areas of knowledge and generate, develop and evaluate ideas andinformation so as to apply these skills to the project task.
- Habituated to critical thinking and use problem-solving skills.
- Communicate effectively and to present ideas clearly and coherently in both written and oral forms.
- Work in a team to achieve a common goal.
- Learn on their own, reflect on their learning and take appropriate actions to improve it.

CIE procedure for Mini - Project:

The CIE marks awarded for Mini - Project, shall be based on the evaluation of Mini - Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25.The marks awarded for Mini - Project report shall be the same for all the batch mates.

M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)SEMESTER -III

INTERNSHIP

Course Code	22LVSI36	CIE Marks	40
Number of contact Hours/Week		SEE Marks	60
Credits	06	Exam Hours	03

Course objectives:
Internship/Professional practice provide students the opportunity of hands-on experience that include personaltraining, time and stress management, interactive skills, presentations, budgeting, marketing, liability and risk management, paperwork, equipment ordering, maintenance, responding to emergencies etc. The objectives arefurther,

- To put theory into practice.
- To expand thinking and broaden the knowledge and skills acquired through course work in the field.
- To relate to, interact with, and learn from current professionals in the field.
- To gain a greater understanding of the duties and responsibilities of a professional.
- To understand and adhere to professional standards in the field.
- To gain insight to professional communication including meetings, memos, reading, writing, publicspeaking, research, client interaction, input of ideas, and confidentiality.
- To identify personal strengths and weaknesses.
- To develop the initiative and motivation to be a self-starter and work independently.

Internship/Professional practice: Students under the guidance of internal guide/s and external guide shall take part in all the activities regularly to acquire as much knowledge as possible without causing any inconvenience atthe place of internship.
Seminar: Each student, is required to

- Present the seminar on the internship orally and/or through power point slides.
- Answer the queries and involve in debate/discussion.
- Submit the report duly certified by the external guide.
- The participants shall take part in discussion to foster friendly and stimulating environment in which thestudents are motivated to reach high standards and become self-confident.

Course outcomes:
At the end of the course the student will be able to:

- Gain practical experience within industry in which the internship is done.
- Acquire knowledge of the industry in which the internship is done.
- Apply knowledge and skills learned to classroom work.
- Develop a greater understanding about career options while more clearly defining personal career goals.
- Experience the activities and functions of professionals.
- Develop and refine oral and written communication skills.
- Identify areas for future knowledge and skill development.
- Expand intellectual capacity, credibility, judgment, intuition.
- Acquire the knowledge of administration, marketing, finance and economics.
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Continuous Internal Evaluation
CIE marks for the **Internship/Professional practice report (20 marks), seminar (10 marks) and question and answer session (10 marks)** shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session by the student) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculty from the department with the senior most acting as the Chairperson.

Semester End Examination
SEE marks for the **internship report (30 marks), seminar (20 marks) and question and answer session (10 marks)** shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session) by the examiners appointed by the University

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M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)
Choice Based Credit System (CBCS) and Outcome Based Education(OBE)SEMESTER -IV

PROJECT WORK PHASE -2

Course Code	22LVS41	CIE Marks	100
Number of contact Hours/Week(L:T:P)	0:0:08	SEE Marks	100
Credits	18	Exam Hours	03

Course objectives:

- To support independent learning.
- To guide to select and utilize adequate information from varied resources maintaining ethics.
- To guide to organize the work in the appropriate manner and present information (acknowledging thesources) clearly.
- To develop interactive, communication, organization, time management, and presentation skills.
- To impart flexibility and adaptability.
- To inspire independent and team working.
- To expand intellectual capacity, credibility, judgment, intuition.
- To adhere to punctuality, setting and meeting deadlines.
- To instil responsibilities to oneself and others.
- To train students to present the topic of project work in a seminar without any fear, face audience confidently, enhance communication skill, involve in group discussion to present and exchange ideas.

Project Work Phase - II: Each student of the project batch shall involve in carrying out the project work jointly
in constant consultation with internal guide, co-guide, and external guide and prepare the project report as per thenorms avoiding plagiarism.

Course outcomes:

At the end of the course the student will be able to:

- Present the project and be able to defend it.
- Make links across different areas of knowledge and to generate, develop and evaluate ideas andinformation so as to apply these skills to the project task.
- Habituated to critical thinking and use problem solving skills
- Communicate effectively and to present ideas clearly and coherently in both the written and oral forms.
- Work in a team to achieve common goal.
- Learn on their own, reflect on their learning and take appropriate actions to improve it.

Continuous Internal Evaluation:

Project Report: 20 marks. The basis for awarding the marks shall be the involvement of the student in the project and in the preparation of project report. To be awarded by the internal guide in consultation with externalguide if any.

Project Presentation: 10 marks.

The Project Presentation marks of the Project Work Phase -II shall be awarded by the committee constituted forthe purpose by the Head of the Department. The committee shall consist of three faculty from the department with the senior most acting as the Chairperson.

Question and Answer: 10 marks.

The student shall be evaluated based on the ability in the Question and Answer session for 10 marks.

Semester End Examination

SEE marks for the project report (30 marks), seminar (20 marks) and question and answer session (10 marks) shall be awarded (based on the quality of report and presentation skill, participation in the question and answer session) by the examiners appointed by the University.